Volume 15, Number 3, 2022. pp. 279-288

Jordan Journal of Physics

ARTICLE

I-V Characteristics Modeling of the Carbon Nanotube Field Effect Transistor (CNTFET)

Siham Kattar and **SaadEddine Khemissi**

Laboratory of Engineering and Sciences of Advanced Materials (ISMA), Faculty of Science and Technology, University of Abbes Laghrour, 40000 Khenchela, Algeria.

Doi: **https://doi.org/10.47011/15.3.6**

Received on: 17/10/2020; *Accepted on: 24/02/2021*

Abstract: A simulation model of a zig-zag type (10.0) single-walled carbon-nanotube (SW-CNT) transistor based on virtual source (VS-CNTFET) approach is presented in this paper. This semi-empirical physics-based model allowed the study of current-voltage (I-V) characteristics of the transistor. Additionally, analytical modeling of reflection coefficient, electron mobility in the CNT with low and high electric field and parasitic resistances (R_s and R_d) were presented as well in this model. Then, the obtained I-V characteristics of this SW-CNTFET were explored and compared with literature data obtained experimentally. Results showed that this model was a different approach which is significant compared to the silicon model in terms of the carrier mobility, where $\mu_{CNT} = 10^4$ cm^2/Vs. Moreover, the impacts of some geometric parameters, such as CNT length and diameter as well as oxide permittivity on the I-V characteristics, were proved.

Keywords: Carbon nanotube, Virtual source, CNTFET, Electron mobility, I-V characteristics.

Introduction

Carbon nanotubes (CNTs) which were invented in 1991have gained much interest as promising materials due to their unique properties [1]. CNTs are known to have high electrical and thermal conductivity, high mechanical properties, high melting point and the ability to be grown on different substrates [2,3]. In particular, their length/diameter aspect ratio provides a high surface/volume ratio. In addition, they are outstandingly able to promote fast electron transfer kinetics for a wide range of electro-active species (like hydrogen peroxide or NADH). Besides, CNTs chemically functionalized can be used to attach almost any desired chemical species to them and make the realization of composite electrodes, comprising having them well-dispersed in an appropriate polymer matrix [4].

CNTs consist of single layers of graphene rolled into a tube shape. They may be single-walled (SWCNTs), consisting of just one rolled sheet, or multi-walled (MWCNTs), having multiple tubes nested within one another [5].

In recent years, potential applications of these nanocomposites have extended to many areas, such as analytical chemistry, electronics and medicine [4]. They are used in devices, such as high-frequency electronics, drug and vaccine delivery vehicles, catalysts for fuel cells, logic gates, sensors and transistors [6–9].

CNTs have greatly impacted the field of semiconductor science, where they are used to provide new field-effect transistors (CNTFETs) [10–13]. CNTFETs that are based on semiconductor of single-wall carbon nanotubes (SW-CNTs) as a channel material are a

Corresponding Author: Siham Kattar **Email**: sihamkattar@gmail.com

promising alternative material to replace silicon in nanoelectronics [14]. Theoretical works on electronic transport through CNTs giving rise to results consistent with experimental data are indeed insufficient in the literature [15]. Therefore, a theoretical study of electronic transport in CNTs is required, as well as modeling and simulation of the static and dynamic characteristics of carbon nanotube components, in order to optimize and improve their performance. Several models, such as compact, analytical and semi-empirical models, were employed to evaluate the impact of physical phenomena, to create a new range of devices in order to design efficient systems [16,17].

In this work, a semi-empirical simulation model called "virtual source (VS-CNTFET) model" was applied to study the I-V characteristics of the CNTFET transistor as well as the effect of physical parameters on these characteristics.

Simulation Model

Simulation of a zig-zag type (10.0) single-walled carbon-nanotube (SW-CNT) transistor (with d=0.78 nm) [18] was based on the so-called "virtual source (VS-CNTFET) model" using Fortran 90 software [19].This semi-empirical physics-based model was originally developed for short-channel Si MOSFETs that have a gate-controlled source-injection barrier [20,21]. Later, the model allowed the description of the I-V characteristics of the studied CNTFET transistors [22,23]. The virtual source name was directly related to the behavior of electronic transport in the channel, since the carriers (electrons or holes) that cross this barrier contribute to the current.

In this model, reflection coefficient was introduced as the ratio of backscattered flow of carriers injected into the channel [20-24]. Then, carrier mobility in carbon nanotubes was used and has been varied. The electron mobility of the silicon-based model (μ_0 ~1250 cm^2/Vs) was replaced by that of CNT at low electric fields (μ_0~10^4 cm^2/Vs). Herein; it was obtained using Eq. (2).

The model was based on the quasi-ballistic transport of electrons in the transistor channel (CNT) and it took into account the effect of the parasitic resistances R_s and R_d at the CNT limitations on the source and drain sides.

Modeling the CNTFET

CNTFET Structure

Fig. 1 represents the scheme of the geometrical structure of a planar CNTFET. The structure is similar to that of the MOSFET (Metal Oxide Semiconductor Field Effect *Transistor*), where the conductor channel in the MOSFET is replaced by a semiconductor CNT in the CNTFET. The CNTFET is a simple device made with the following architecture:

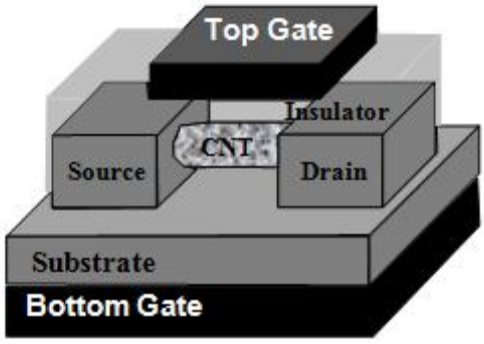

FIG. 1. Planar structure of a carbon nanotube field effect transistors (CNTFET) used for simulation [22].

A semiconductor of carbon nanotubes formed the channel deposited on a doped substrate; an oxide of thickness t_{ox} was placed between two metal electrodes, taking the names of drain (D) and source (S), respectively; if a voltage V_{DS} was applied between the drain and the source electrodes, an electric field was created by imposing a potential difference V_{GS} between the gate (G) and the doped substrate, a current I_{DS} circulating between the source and the drain was measured as a function of V_{DS} and V_{GS}.

Mobility Model

In semiconductors, the relationship between the carrier velocity and the electric field is expressed as:

$$v(E) = \mu(E) \quad (1)$$

where *v(E)* is the carrier velocity, E is the electric field and $\mu(E)$ is the carrier mobility (electrons or holes).

The law of the carrier mobility as a function of the electric field can be expressed as follows:

For low electric fields:

$$\mu(E) = \mu_0$$

with:

$$\mu_0 = \frac{q\tau}{m^*} \quad (2)$$

where $m*$ is the effective mass, which is inversely proportional to the diameter d [25,26].

$$m^* = \frac{2\hbar^2}{3v_f d} \quad (3)$$

v_f is the Fermi velocity,

$$v_f = 8.\,10^5\ m.s^{-1} \quad (4)$$

and d is the diameter of the CNT.

The relaxation time is given by the following expression [27–29]:

$$\tau = \frac{d}{\alpha T}\ . \quad (5)$$

The expression of mobility most noticeable is given as below [30]:

$$\mu = \frac{\mu_0}{(1+(E/E_C)^\gamma)^{1/\gamma}} \quad (6)$$

$$E_C = \mu_0\ /v_{sat} \quad (7)$$

γ is given in [31] by:

$$\gamma = 1 - 2.8 \quad (8)$$

where: v_{sat} is the saturation velocity and E_C represents the critical electric field. In our model, the mobility reaches a value different from that of silicon.

$(\mu_{0(CNT)})$= 10^4 cm^2/Vs [32],

$\mu_{0(Si)}$ = 1250 cm^2/Vs.

It is known that the efficiency of shocks increases with the energy of electrons. For the population as a whole, this increases the non-linear variation in stationary velocity as a function of the electric field intensity.

The evolution of the electron velocity as a function of the electric field was calculated using Eqs. (1) and (2) and is presented in Fig. 2. In the case of intrinsic CNT (10.0), it was noticed that the curve could be divided into two regimes; the linear regime where the velocity increased linearly with the electric field to a critical point E_C, as well as the saturation regime starting at v_{sat}.

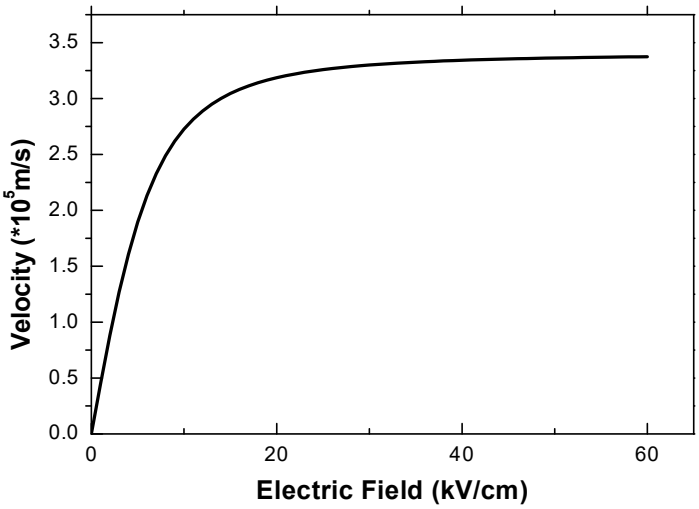

FIG. 2. Characteristics of the electron velocity as a function of the electric field.

I-V Characteristic

In virtual source modeling [33–35], the total flow of the source and drain contributions can be written as follows:

$$F_S^- = R.F_S^+ + (1-R).F_d^+ \quad (9)$$

where: F_S^+ (respectively F_d^+) is the flux injected by the source (respectively the drain) in the case where the contacts are ideal.

In this case, the expressions of the inversion charge in the CNT are given as follows:

$$Q_{inv} = \frac{q}{v_{th}}(F_S^- - F_S^+) \quad (10)$$

$$Q_{inv} = C_{OX}(V_G - V_t) \quad (11)$$

$$C_{OX} = \frac{2\pi\varepsilon}{log(2t_{ox}/d)} \quad (12)$$

V_G is the gate voltage, V_t is the threshold voltage and C_{OX} is the oxide capacity.

The thermal velocity is given by:

$$v_{th} = v_{sat}F_S \quad (13)$$

$$F_S = \frac{(V_D/V_{Dsat})}{(1+(V_{DS}/V_{Dsat})^{\beta})^{1/\beta}} \quad (14)$$

β is a constant (β =*1.8*) [20].

If we consider that the average carriers' velocities coming from the source or the drain are identical, the expression of the current becomes:

$$I_D = qW(F_S^- + F_S^+) \quad (15)$$

with: W is the width of the CNTFET and q is the elementary charge.

In the non-degenerate case [33,35], the flow of the carriers from the drain is equal to:

$$F_D^+ = F_S^+ e^{\frac{-qV_D}{k_B T}} \quad (16)$$

Using Eqs. (10), (13) and (15), we can then express the quasi-ballistic current in the non-degenerate case as follows:

$$I_D = Q_{inv} v_{th} W \frac{(1-R)}{(1+R)} \left(\frac{(1-exp(-qV_D/k_BT)}{1+\left(\frac{(1-R)}{(1+R)}(1-exp(-qV_D/k_BT)\right)} \right) \quad (17)$$

with: k_B is the Boltzmann constant and R is the reflection coefficient:

$$R = \frac{L}{(L+\lambda)} \quad (18)$$

λ is a constant and L is the length of the carbon nanotubes.

The drain-induced barrier lowering (DIBL) is given as [20]:

$$DIBL = e^{-\eta} \quad (19)$$

with:

$$\eta = \frac{L+2L_{of}}{2\lambda} \quad (20)$$

and:

$$L_{of} = t_{ox}/3 \quad (21)$$

And the sub-threshold swing SS is defined as [20]:

$$SS = n_{ss}(ln10.k_B.T/q) \quad (22)$$

where:

$$n_{ss} = \frac{1}{1-e^{-\eta}} \quad (23)$$

Effect of Parasitic Resistances R_s and R_d

The previously presented expression in (17) of the drain current was calculated on the basis of the intrinsic quantities (I_D, V_D and V_G), without taking into consideration the access resistances' effect on the source and drain sides (R_s and R_d, respectively). These resistances resulted in extensions between the gate and source electrodes for R_s and between the gate and drain electrodes for R_d, in addition to contacts between the sources, drain metals and the semiconductor (CNT). To obtain the expressions of the measurable quantities (I_{DS} as a function of V_{DS} and V_{GS}), the following modifications were introduced on the expression in (17) of the drain current:

$$\left.\begin{aligned} V_{GS} &= V_G + R_s.I_D \\ V_{DS} &= V_D + (R_s + R_d).I_D \\ I_{DS} &= I_D \end{aligned}\right\} \quad (24)$$

Results and Discussion

To exploit the mathematical model, Fortran 90 software was used to solve the system of mathematical equations and to plot the curves.

The simulation was performed on a CNTFET transistor with the following parameters:

TABLE 1. Parameters of the zig-zag type (10.0) (SW-CNT) transistor.

Gate length L (nm)	80
Diameter of CNT d (nm)	0.78
Ambient temperature T(K)	300
Threshold voltage V_t (V)	0.1
Relative permittivity of the oxide ε_r	2.4
Thickness of oxide t_{ox} (nm)	1.5
Mobility of electrons μ_0 (cm^2/ Vs)	10000
λ (nm)	66.2
γ	2

In Fig. 3, the I-V characteristics for the device were presented with two gate lengths, the first length L = 50 nm and L = 80 nm for the second, at different gate voltages (V_{GS} = 0.2, 0.4, 0.6 and 0.8 V). Noticeably, the saturation regime was not stable; it increased slightly with the increase in the drain voltage (calculated and shown for the three voltage values and two different devices). In addition, the current in the transistor with L = 50 nm was greater than in the second case with L = 80 nm for all values of V_{DS} and V_{GS}. This explained the importance of reducing the gate length as much as possible to have better I-V characteristics for all FET devices.

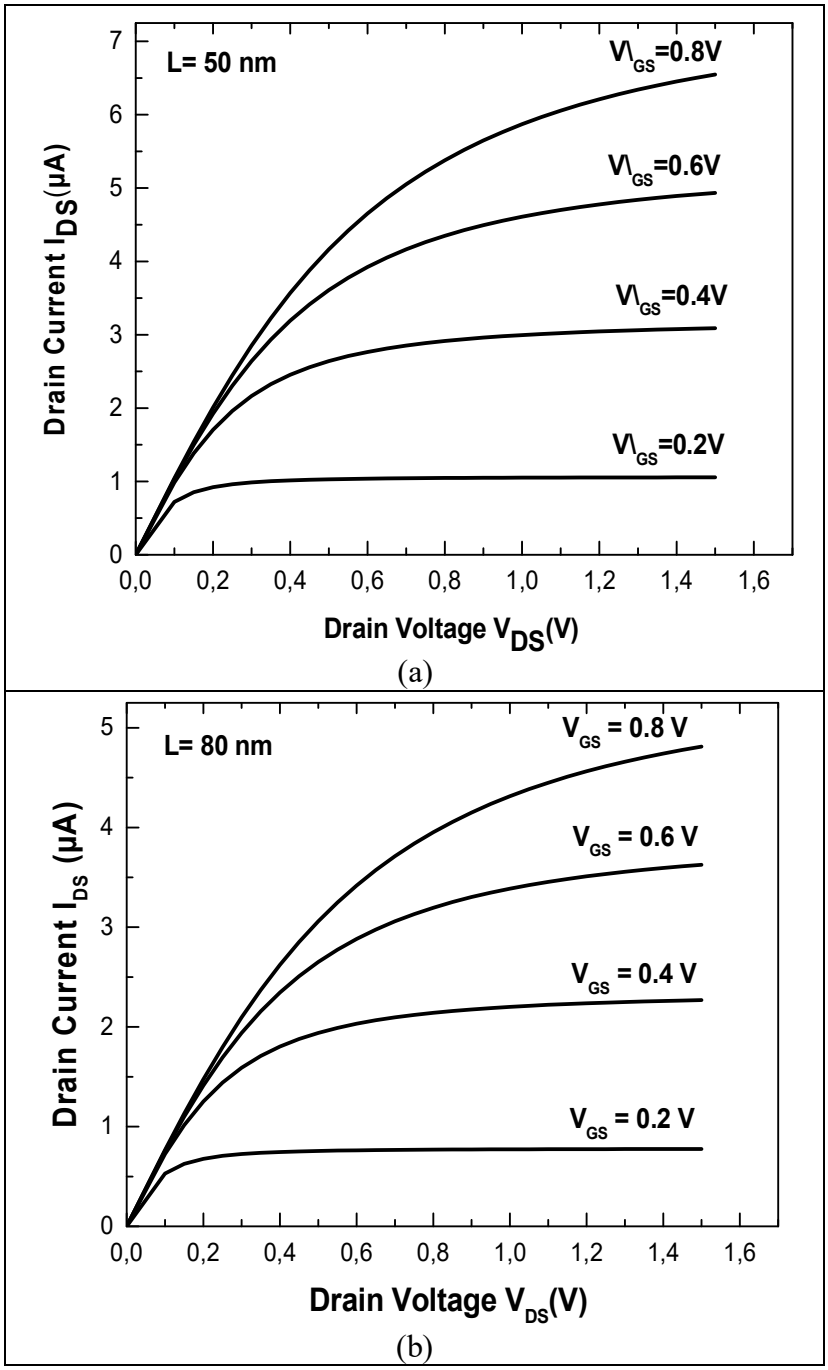

FIG. 3. I-V characteristics of (a) the first CNTFET with gate length L = 50 nm and (b) the second CNTFET with gate length L = 80 nm.

Fig. 4 depicts the variation of the drain current as a function of the gate voltage for three values of drain voltage (V_{DS} = 0.6 V, 1.2 V and 1.8 V) for the first device with L = 50 nm. From this figure, the drain current showed an increase with increasing gate voltage and the drain current appeared from a gate voltage value (V_{GS} = 0.1 V) for the three values of the drain voltage. This value represented the threshold voltage for this device.

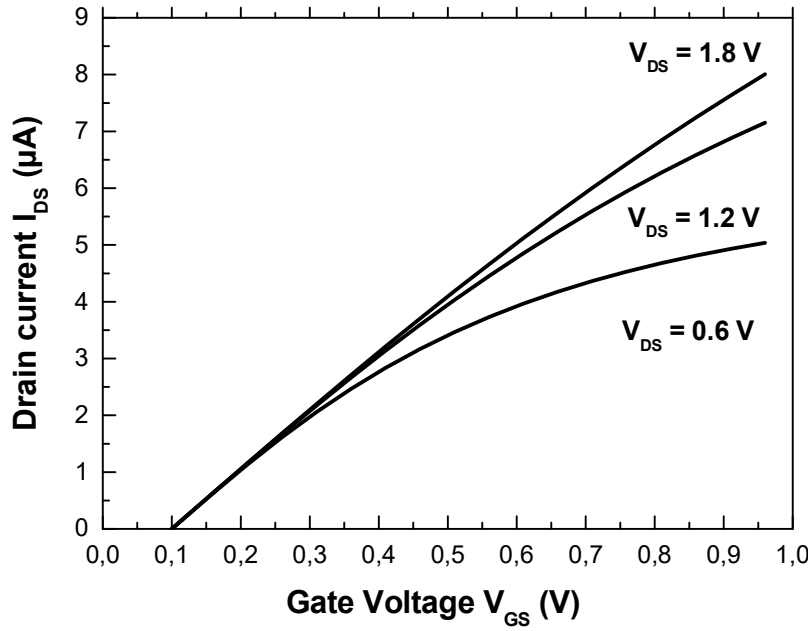

FIG. 4. I_{DS}–V_{GS} characteristics for V_{DS} = 0.6 V, V_{DS} = 0.8 V and V_{DS} = 1.2 V with gate length L = 80 nm.

In Fig. 5, the characteristics of the drain current for different values of the gate length (L= 30, 50 and 80 nm) were presented. It can be seen that the drain current intensity increased with the decrease in the gate length; this characteristic was corresponding to all the FET transistors.

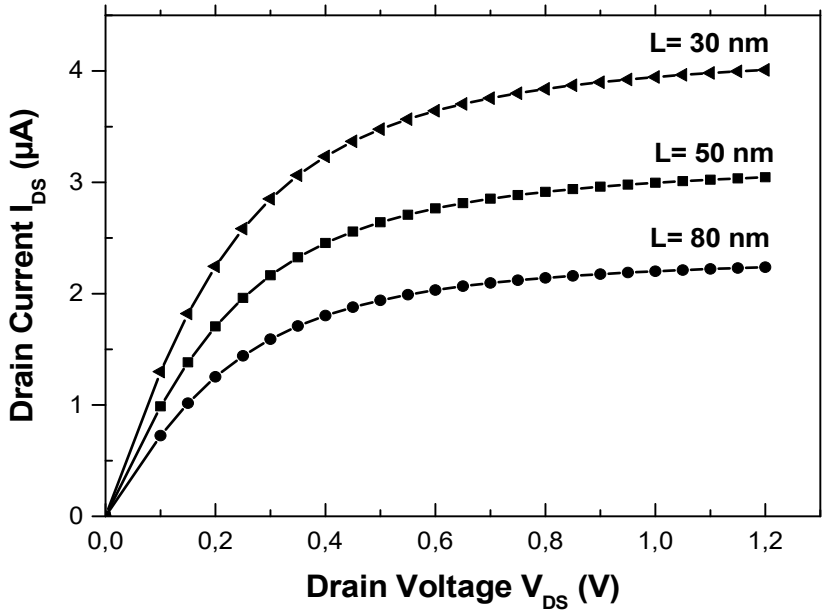

FIG. 5. Effect of CNT length on drain current I_{DS} for different gate lengths (L).

Fig. 6 shows the drain current variations as a function of the drain voltage for different diameters of the CNT. It was noticed that the drain current was very sensitive towards the values of the carbon nanotube diameters. For example, the saturation current passed from 4.3 μA to 14.4 μA when the diameter of the CNT went from 0.78 nm to 2 nm.

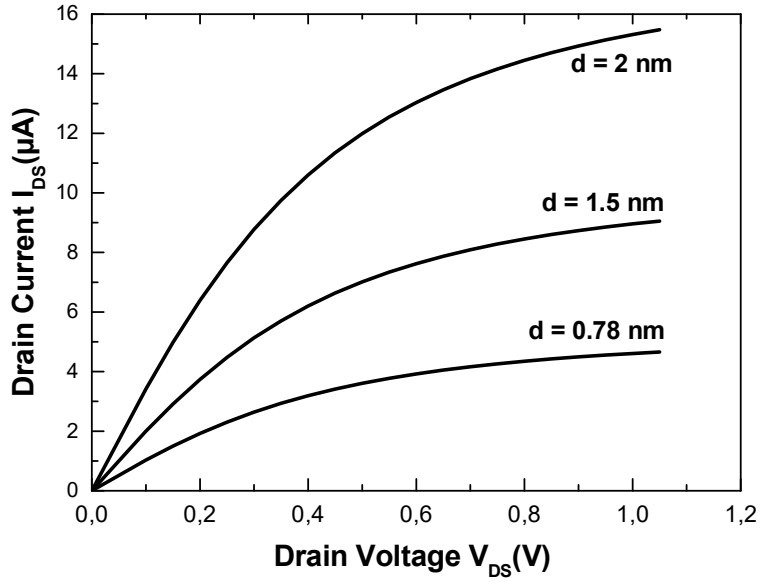

FIG. 6. I_{DS}–V_{DS} characteristics for CNT diameters (d = 0.78 nm, d = 1.5 nm and d = 2 nm).

In order to demonstrate the effect of parasitic resistances R_s and R_d on the I-V characteristics of the SW-CNTFET (with V_{GS} = 0.4 and 0.8 V) [35], variations of the drain current as a function of the bias voltages with and without the parasitic resistances are shown in Fig. 7. It is clear that the effect of these resistances cannot be neglected, because the essential effect of parasitic resistances decreases the potential applied to the sides of the active area. This difference is approximately 20% of the intrinsic value and it is of more obvious influence when the drain current "I_{DS}" is high.

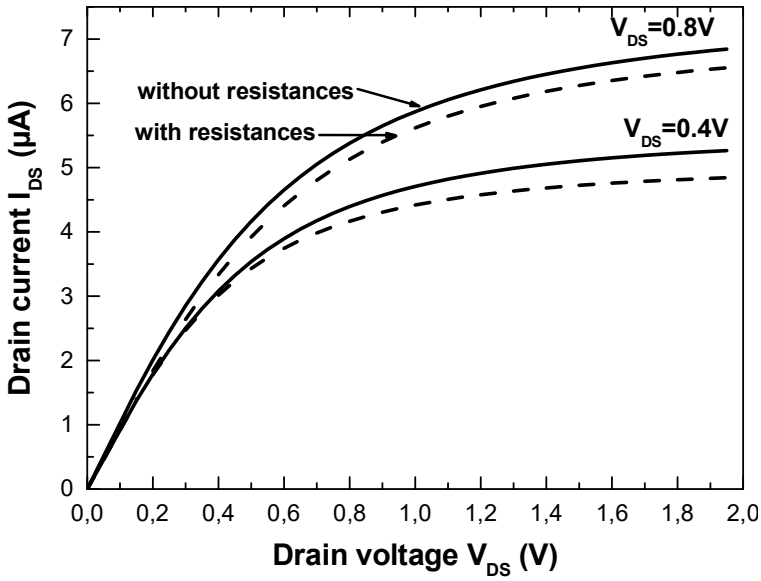

FIG. 7. Parasitic resistances' effect on the I_{DS}-V_{DS} curve with R_s=R_d = 4.5 kΩ, V_{GS}= 0.4 V and V_{GS}= 0.8 V.

The DIBL variations as a function of the gate length for three different oxide thicknesses (t_{ox}= 1.5 nm, t_{ox}= 6 nm and t_{ox}= 10 nm) are demonstrated in Fig. 8. The DIBL decreases with increasing the gate length.

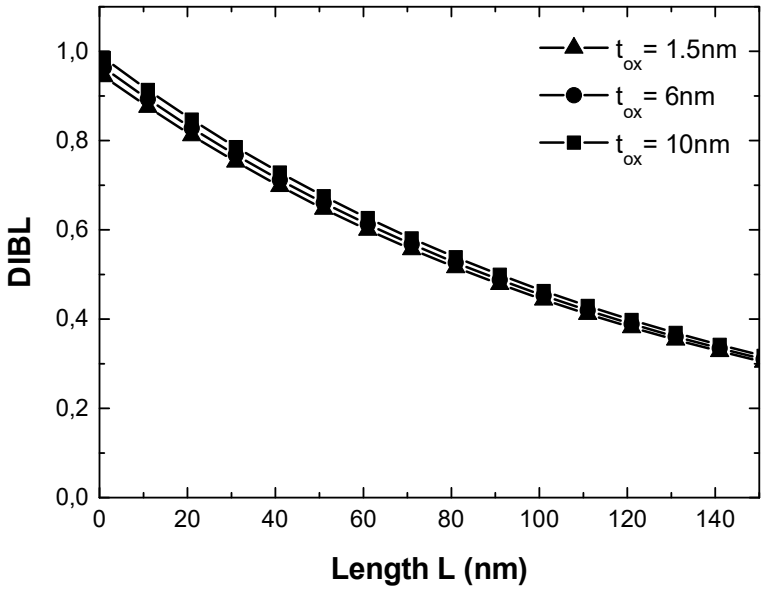

FIG. 8. Drain-induced barrier lowering (DIBL) *versus* CNT length with different oxide thicknesses t_{ox}= 1.5 nm, t_{ox}= 6 nm and t_{ox}= 10 nm.

Fig. 9 shows the sub-threshold slope variations (SS) as a function of the gate length for different oxide thicknesses (t_{ox} = 2 nm, t_{ox} = 5 nm and t_{ox} = 7nm). It was evidenced that the SS varied with the oxide thickness, where it raised up by the increase of the oxide thickness and decreased by the gate-length increase.

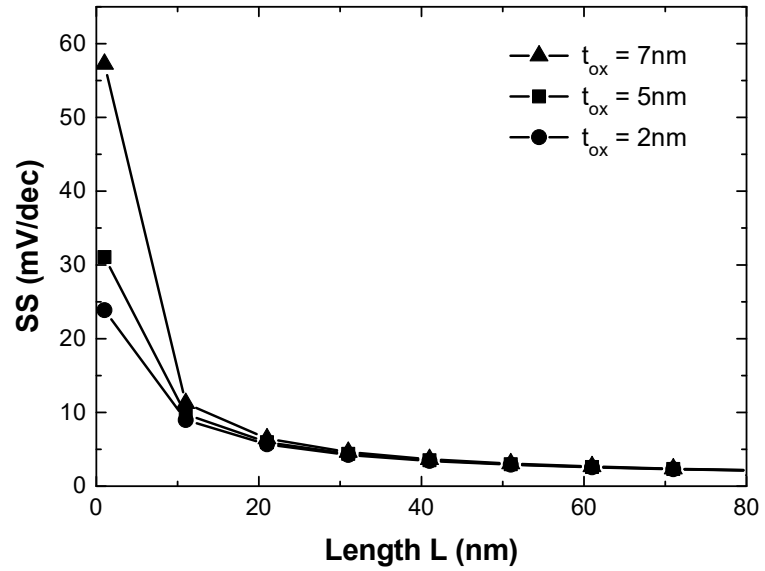

FIG. 9. Sub-threshold slope (SS) *versus* CNT length (L) with different oxide thicknesses t_{ox}= 2 nm, t_{ox}= 5 nm and t_{ox}= 7 nm.

In order to examine the validity of the exposed model, Fig. 10 presents a comparison between the results obtained from our model and the experimental data given by Lee et al. in [23]. Here, the ellipse shape is used to indicate that the comparison (I_{DS}-V_{DS}) between our model (small triangles) and experimental results (small circles) is given at a value of grid voltage V_{GS}. For example, the first two comparison curves represent the (I-V) characteristics for V_{GS} = 0.8V.

The I_{DS}-V_{DS} characteristics of a CNTFET with gate length L_g = 15 nm at V_{GS} (0.8, 1.0 and 1.2 V) are presented, where good agreement between the results is observed, especially for V_{GS} less than 2.0 V; but even for V_{GS} greater than 2.0 V The two works still have an acceptable agreement, which proves the validity of the proposed model.

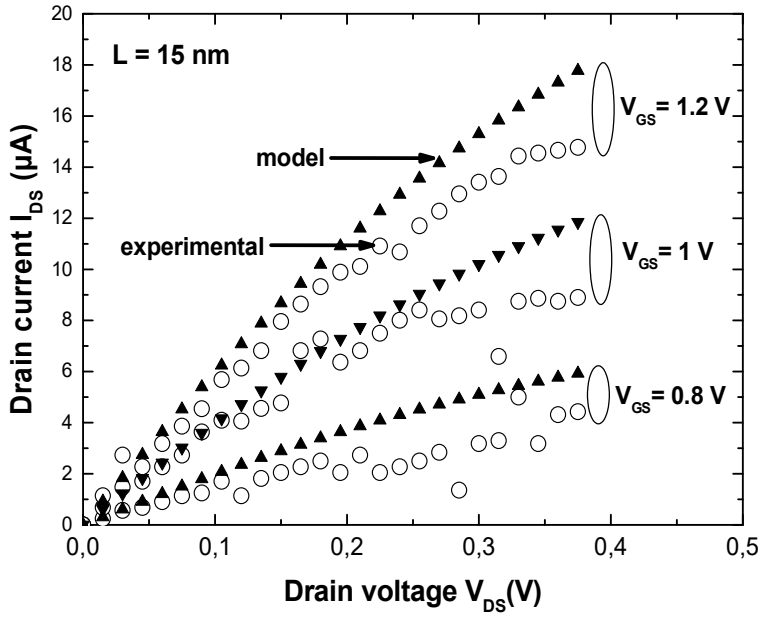

FIG. 10. Comparison between the I-V characteristics from the proposed model (small triangles) and experimental data (small circles) given by [23] for a CNTFET with L_g = 15 nm.

Conclusion

A semi-empirical model on "virtual source (VS-CNTFET) model" using Fortran 90 software was presented for the description of I-V characteristics of a zig-zag type (10.0) single-walled carbon-nanotube (SW-CNT) transistor (with d= 0.78 nm). The simulation model was based on reflection coefficient as the ratio of backscattered flow of carriers injected into the channel. Moreover, the electron mobility value used in this model is that of CNTs at low electric fields (μ_0=10^4 cm^2/Vs), unlike most other models using electron mobility in silicon (μ_0 =1250 cm^2/Vs). In addition, the effects of parasitic resistances R_s and R_d at the CNT limitations on the source and drain sides have not been neglected. This study made it possible to highlight the influence of the reflection coefficient that must be integrated in quasi-ballistic transport, as well as at the low-field electron mobility of carbon nanotubes. In the quasi-ballistic transfer, electrons undergo interactions, while in ballistic transport, electrons do not undergo any interaction, where the charge carriers cross the channel to contribute to the current. Therefore, it was necessary to introduce the concept of reflection as being the ratio of backscattered flows to carrier-injected flows. This concept is the coefficient of reflection and that is negligible in ballistic transfer.

In our work, CNT electron mobility was calculated and matched with the value reported in literature μ_{CNT} = 10^4 cm^2/Vs. The main results of I-V characteristics of the SW-CNT transistor-based model were established based on the following points: first, the importance of reducing the gate length (better with L=50 nm) as much as possible for all FET devices. Additionally, a gate voltage V_{GS} of 0.1 V represented the threshold voltage for the device. Moreover, the drain current intensity was related to the gate length and carbon nanotube diameter. Taking parasitic resistances into account, they have a non-negligible effect. Clearly, the DIBL decreased when the gate length increased. Finally, the sub-threshold slope (SS) varied with oxide thickness and gate length variation. Results of this work confirmed the validity of the simulation method, being in good agreement with those obtained experimentally and reported in literature [23].

References

[1] Iijima, S., Nature, 354 (1991) 56.

[2] Yun, Y. H., Shanov, V., Schulz, M.J., Dong, Z., Jazieh, A., Heineman, W.R., Halsall, H.B., Wong, D.K.Y., Bange, A., Tu, Y. and Subramaniam, S., Sen. A. Chem. B, 120 (2006) 298.

[3] Mousa, M.S., Al-Akhras, M.A.H. and Daradkeh, S.I., Jordan J. Phys., 11 (2018) 17.

[4] Wang, J., Musameh, M. and Lin, Y., J. Am. Chem. Soc., 125 (2003) 2408.

[5] Endo, M., Kim, Y.A., Muramatsu, H., Yanagisawa, T., Hayashi, T. and Dresselhaus, M.S., New Diamond and Frontier Carbon Tech., 14 (2004) 1.

[6] Che, G.L., Lakshmi, B.B., Martin, C.R. and Fisher, E.R., Langmuir, 15 (1999) 750.

[7] Postma, H.W.C., Teepen, T., Yao, Z., Grifoni, M. and Dekker, C., Science, 293 (2001) 76.

[8] Bachtold, A., Hadley, P., Nakanishi, T. and Dekker, C., Science, 294 (2001) 1317.

[9] Lim, S.H., Wei, J., Lin, J., Li, Q. and Kua You, J., Biosensors and Bioelectronics, 20 (2005) 2341.

[10] Nasir, S., Hussein, M.Z., Zainal, Z. and Yusof, N.A., Materials, 11(2018) 295.

[11] Mousa, M. S., Daradkeh, S.I. and Bani Ali, E.S., Jordan J. Phys., 12 (2019) 7.

[12] Cao, J., Wang, Q. and Dai, H., Phys. Rev., 90 (2003) 157.

[13] Shiraishi, M., Takenobu, T., Iwai, T., Iwasa, Y., Kataura, H. and Ata, M., Chem. Phys. Lett., 394 (2004) 110.

[14] Marani, R. and Perri, A.G., I. J. Elec., 6 (2013) 1055.

[15] Grado-Caffaro, M.A. and Grado-Caffaro, M., Optik, 115 (2004) 45.

[16] Bandaru, P.R., J. N. N., 7 (2007) 1.

[17] Wind, S.J., Appenzeller, J., Martel, R., Derycke, V. and Avouris, P., A. Phys. Lett., 80 (2002) 3817.

[18] Sahoo, R. and Mishra, R.R., IJEE, 1 (2009) 117.

[19]http://fortran.softwaresea.com/Linux-software-download/fortran-90.

[20] Khakifirooz, A., Nayfeh, O.M. and Antoniadis, D., IEEE TED, 56 (2009)1674.

[21] Dukovic, G., Wang, F., Song, D., Sfeir, M.Y., Heinz, T.F. and Brus, L.E., Nano-Lett., 5 (2005) 2314.

[22] Luo, J., Wei, L., Lee, C.S., Franklin A.D., Guan, X., Pop, E., Antoniadis, D.A. and Wong, H.S., IEEE TED, 60 (2013) 1834.

[23] Lee, C., Pop, E., Franklin, A.D., Haensch, W. and Wong, H.P., IEEE TED, 62 (2015) 3061.

[24] Lundstrom, M.S. and Antoniadis, D.A., IEEE TED, 61 (2014) 225.

[25] Saito, R., Dresselhaus, G. and Dresselhaus, M.S., "Physical Properties of Carbon Nanotubes", Edn. (2), (Imperial College Press, Tokyo, 1998), p.80.

[26] Zhou, X., Park, J.Y., Huang, S., Liu, J. and McEuen, P.L., Phys. Rev. Lett., 95 (2005) 146805.

[27] Suzuura, H. and Ando, T., Phys. Rev. B, 65 (2002) 235412.

[28] Pennington, G. and Goldsman, N., Phys. Rev. B, 68 (2003) 045426.

[29] Perebeinos, V., Tersoff, J. and Avouris, P., Phys. Rev. Lett., 94 (2005) 086802.

[30] Greenberg, D.R. and del Alamo, J.A., IEEE TED, 41 (1994) 1334.

[31] Chek, D.C.Y., Tan, M.L.P., Ahmadi, M.T., Ismail, R. and Arora, V.K., J. Micro-elec., 41 (2010) 579.

[32] Dürkop, T., Getty, S.A., Cobas, E. and Fuhrer, M.S., Nano-Lett., 4 (2004) 35.

[33] Martinie, J.S., Vedraine, S., Munteanu, D., Le Carval, G. and Barral, V., Proc. Fringe-ESSDERC, Edinburgh, Scotland (2008).

[34] Martinie, D.S. and Anu, G., Proc. JNRDM (2007).

[35] Lundstrom, M., "Fundamentals of Carrier Transport", Edn. (2), (Cambridge University Press, Cambridge, 2000), p.440.