Volume 17, Number 4, 2024. pp. 483-495

Jordan Journal of Physics

ARTICLE

Simulated Transimpedance Amplifier Performance Analysis through Channel Length Modification for Fiber Optics Applications

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Doi: **https://doi.org/10.47011/17.4.11**

Received on: 01/04/2023; *Accepted on: 07/06/2023*

Abstract: A proposed transimpedance amplifier was simulated using channel length modification. The amplifier consists of a feedforward input stage followed by a common gate-common source (CG-CS) configuration. A series of channel lengths (45, 90, and 130 nm) in complementary metal-oxide semiconductor (CMOS) technology was implemented for comparative performance analysis within the same proposed topology. There are two key advantages of this study. First, the trade-off between gain and bandwidth, as well as the input-referred noise current, remains applicable when the channel length is increased from 45, 90, and 130 nm. Second, power consumption decreases as the channel length increases for the same topology. The total power consumption series (0.621, 0.29, and 0.175 mW) corresponds to the above channel length series. Corresponding bandwidths of (1.69, 1.35, and 1.10 GHz) were reported, with respective transimpedance amplifier (TIA) gains of (44.78, 46.39, and 47.94 dBΩ). The input-referred noise current was reduced to (15.24, 10.77, and 9.40 $pA/\sqrt{H_z}$) for the channel lengths of 45, 90, and 130 nm, respectively, aligning with the trends observed in bandwidth and TIA gain.

Keywords: Transimpedance amplifier, Feedforward, Front-end preamplifier, RGC.
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PACS: 85.40.-e, 07.50.Ek, 84.30.-r.

1. Introduction

Fiber optic networks are meeting the demands for high-speed (Gb/s) systems of communications which are rapidly growing. A comparative analysis of a transimpedance amplifier (TIA) using 45 and 180 nm inductorless CMOS process was achieved in which a single-ended current-mode TIA in the form of N similar TIAs in parallel configuration was conducted [1]. A 45 nm silicon-on-insulator (SOI) CMOS process was demonstrated in the form of a 40 Gb/s optical transceiver that consists of a TIA where a feedback resistor is connected between the gate and drain of NMOS and PMOS transistors [2]. A two-phase TIA was implemented in 45 nm CMOS, featuring a regulated cascode (RGC) and an inverted cascode output stage [3]. A 5 Gbps TIA in a 90 nm CMOS process that employs an active RGC structure at the input stage leading to low input resistance which was followed by a level shifter and a common source structure to achieve high transimpedance at low supply voltage was introduced [4]. A modified RGC TIA followed by a closed loop gain stage with an added level shifter circuit to the booster of a conventional RGC circuit was proposed in the 90 nm CMOS process [5]. A TIA with three cascaded stages in the form of common source amplifiers utilizing capacitive degeneration and inductive peaking in a 90 nm CMOS process was introduced [6]. A conventional RGC TIA employing a cascode inverter as proposed local feedback was implemented in 130 nm CMOS technology [7]. A 2.5 Gbit/s TIA was realized in 130 nm CMOS technology that involved using a common source (CS) amplifier with active inductive peaking [8].

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A 64-Gbaud TIA in 130 nm SiGe process was implemented. The topology involved a π–network broadband technique and shunt-shunt RC feedback to achieve high gain and a wide bandwidth [9]. A double cascode TIA with inductive peaking and shunt-shunt negative feedback was realized in a 130 nm RF CMOS process for 10 Gbps optoelectronic receivers [10].

1.1 Feedforward Transimpedance

The common gate topology of transistor M_2 enables it to function as a source follower because it is a part of a feedback loop, as illustrated in Fig. 1(a). At low frequencies, resistor R_2 is comparable to the total TIA gain. The input resistance is represented by Eq. (1) [11], if the loop at the M_2 gate is broken, and assuming that body effect and channel length modulation are disregarded:

$$R_{in} = \frac{1}{g_{m2}}\left(\frac{1}{1+g_{m1}R_1}\right) \quad (1)$$

where g_{m1} and g_{m2} are the transconductance parameters of transistors M_1 and M_2, respectively. The feedback loop lowers the input resistance, extending the bandwidth as a result. The circuit in Fig. 1(a) can be redrawn as shown in Fig. 1(b), which is essentially a feedforward amplifier that drives the gate of transistor M_2, which is in a common-source formation.

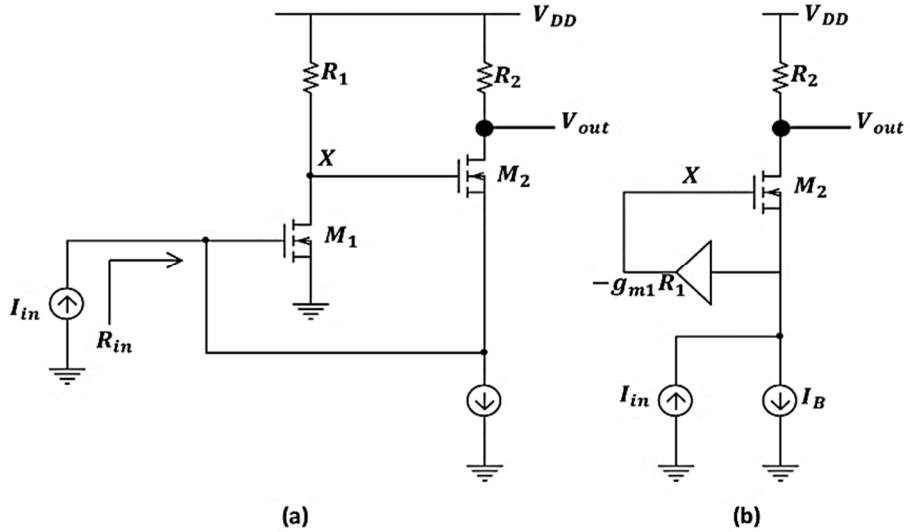

FIG. 1. (a) TIA in a feedback form, (b) Amplifier inserted in feedforward path [11].

1.2 Regulated Cascode TIA

In common-gate (CG) configurations, the impact of large input parasitic capacitance on bandwidth can be mitigated. However, it is difficult to totally isolate this capacitance when the CG topology is used as an input stage. Power consumption constraints also limit the transconductance parameter g_m of the NMOS transistor. The noise performance is normally deteriorated by a small g_m. The RGC input mechanism provides a valuable solution by enhancing g_m effectively. This RGC amplifier input node sits at virtual ground enabling wider bandwidths [12]. The RGC schematic circuit is shown in Fig. 2. where the photodiode current is turned into an amplified voltage at the drain of transistor M_2. Local feedback through transistor M_1 with R_b at its drain reduces input impedance equivalent to the same amount of its own voltage gain. The TIA gain is equal to R_F. The RGC input impedance is $(1 + g_{m1}R_b)$ times smaller than in the CG configuration.

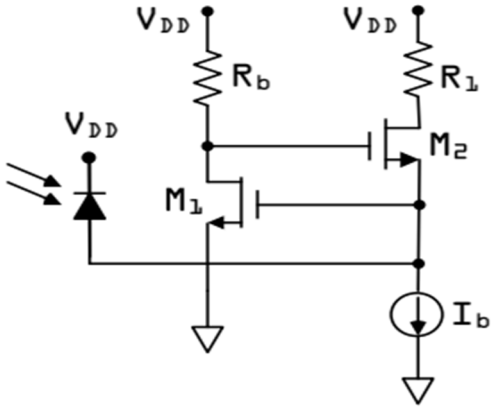

FIG. 2. A typical regulated cascode TIA [12].

The pole in the local feedback of Fig. 2 is a pole zero in the transfer function, leading to frequency peaking at $1/[2\pi R_b(C_{gs2} + C_{db1})]$, where C_{gs2} and C_{db1} are the gate-to-source

capacitance of transistor M_2 and the drain-to-bulk capacitance of transistor M_1, respectively. In order to avoid peaking, two options are possible: either the resistance or the gate width of transistor M_2 can be reduced. When R_b is reduced, then the input transconductance g_m is reduced almost in a linear manner. The input transconductance is reduced at a slower pace when the width of transistor M_2 is decreased. This can lead to an increase in the contribution of channel thermal noise from transistor M_2 as a result of smaller g_{m2} [12]. These RGC configuration challenges are noted in other studies [13-15].

This work aims to investigate the effects of channel length modification on a proposed TIA topology, focusing on the trade-off between gain and bandwidth, input-referred noise, and power consumption reduction as channel length increases.

2. Proposed TIA Topology

The schematic in Fig. 3 illustrates a current gain provider in the form of an input feedforward stage followed by a transimpedance gain provider in a common-gate common-source (CG-CS) arrangement. Nodes X and Y in the input stage must have sufficient voltage headroom to permit a measurable drain current for amplifier transistors M_1 and M_3. The DC level rise at node X through the pass transistor M_2 overcomes this voltage headroom. As a result, transistor M_1's drain-to-source voltage is also given the ability to have sufficient headroom. This input stage setup builds upon previously published designs [16].

As for the CG-CS stage, it is a modified form of the transconductance parameter g_m boosting mechanism. The drain of transistor M_{10} at node B provides enough gate-to-source voltage headroom for transistor M_9. Hence, a boosted g_m for transistor M_9 enables lower input impedance at node $in2$, expanding the bandwidth of the CG-CS stage. Interestingly, the low input impedance of this stage represents a low load for the input feedforward stage. The CS high input impedance at node A is in parallel with the source limited and finite input impedance of transistor M_9.

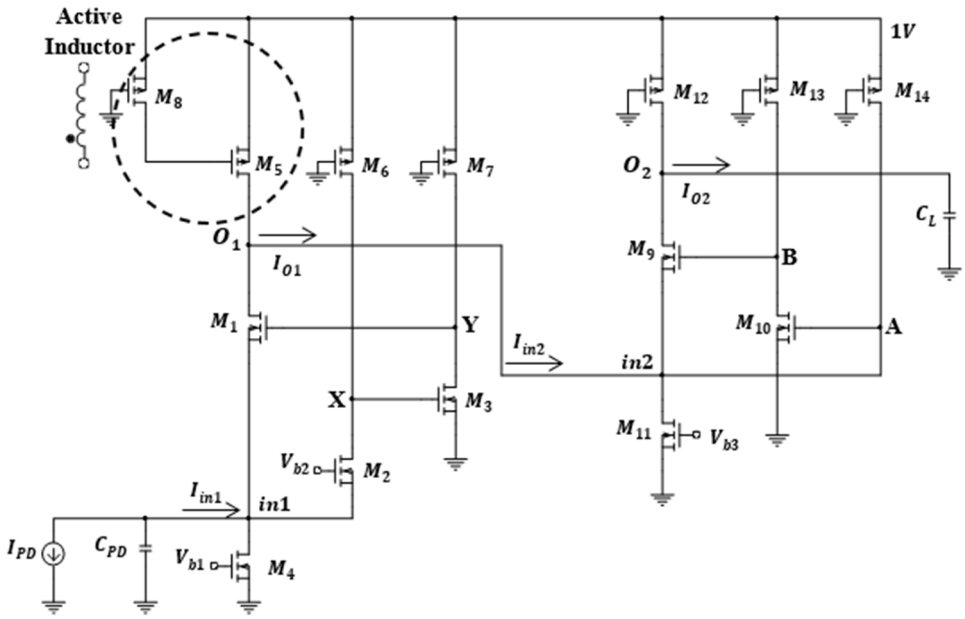

FIG. 3. Proposed TIA topology.

For the input stage, the small signal model is represented in Fig. 4. The input current I_{in1} that enters node $in1$ is a fraction of the photodiode current I_{PD} since some of it vanishes through the photodiode capacitance C_{PD}. The current source as an active inductor impedance is illustrated as Z_{AI}. The drain current of transistor M_1 is governed by the voltage difference between nodes Y and $in1$, while the drain current of transistor M_3 is governed by the voltage swing on node X. Gate biasing for transistor M_4 provides a stable path for drain current o M_1.

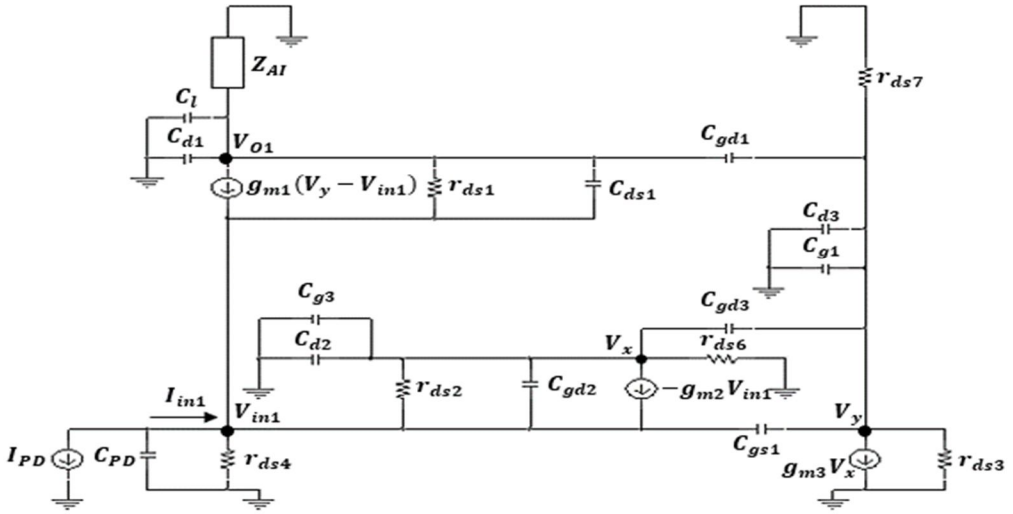

FIG. 4. Small-signal model of the feedforward input stage.

The small-signal model analysis is governed by KCL equations is represented as follows. In this analysis, g_{mx} is the transconductance representation as per numbered transistors, g_{mbx} is the bulk transconductance parameter, g_{dx} is the output conductance, while C_{dx} and C_{gx} are the total drain and gate capacitances, respectively. Gate-to-drain capacitances are given as C_{gdx}, while gate-to-source capacitance is represented as C_{gs1}. The total input capacitance $C_{in,tot1} = C_{PD} + C_{s1} + C_{s2} + C_{d4}$ is dominated by the photodiode capacitance.

$$I_{in1} = V_{in1}\big(g_{m1} + g_{mb1} + g_{ds1} + g_{m2} + g_{mb2} + g_{ds2} + g_{ds4} + sC_{in,tot1}\big) - V_X\, g_{ds2} - V_Y\big(g_{m1} + sC_{gs1}\big) - V_{O1}\, g_{ds1} \quad (2a)$$

$$0 = V_X\left(g_{ds6} + g_{ds2} + s\big(C_{d2} + C_{g3}\big)\right) - V_Y sC_{gd3} - V_{in1}(g_{m2} + g_{mb2} + g_{ds2}) \quad (2b)$$

$$0 = V_Y\left(g_{ds7} + g_{ds3} + s\big(C_{d3} + C_{g1}\big)\right) - V_X\big(g_{m3} - sC_{gd3}\big) - V_{O1}sC_{gd1} - V_{in1}\, s\, C_{gs1} \quad (2c)$$

$$0 = V_{O1}\big(Y_{AI} + g_{ds1} + s(C_{d1} + C_L)\big) + V_Y\big(g_{m1} - sC_{gd1}\big) - V_{in1}(g_{m1} + g_{mb1} + g_{ds1}) \quad (2d)$$

The voltage gain of the input stage circuit is deduced as:

$$A_{v1} = \frac{V_{O1}}{V_{in1}} = \frac{g_{m1}(1+|A_{M2}A_{M3}|)+g_{mb1}+g_{ds1}}{Y_{AI}+g_{ds1}+s(C_{d1}+C_L)} \quad (3)$$

Here, A_{M2} is the voltage gain of transistor M_2 and A_{M3} is the voltage gain of transistor M_3. The active inductor load admittance Y_{AI} is defined through the inversion of active inductor impedance as follows [17]:

$$Z_{AI} = \frac{r_{o8}C_{gs5}s+1}{g_{m5}+C_{gs5}s} \quad (4)$$

From Eq. (3), the TIA gain of the input stage is:

$$Z_{TIA1} = Z_{in1}A_{v1} = \frac{A_{v1}}{P+sC_{eq1}} \quad (5)$$

The input impedance of the input stage is given as:

$$Z_{in1} = \frac{1}{P+sC_{eq1}} \quad (6)$$

where P is worked out as:

$$P = g_{m1}(1 + |A_{M2}A_{M3}|) + g_{ds2}(1 - A_{M2}) + g_{ds1}(1 - A_{v1}) + g_{mb1} + g_{m2} + g_{mb2} + g_{ds4} \quad (7)$$

The equivalent input capacitance is defined as $C_{eq1} = \big[C_{i,tot1} + |A_{M2}A_{M3}|C_{gs1}\big]$, while the output impedance of the input stage is as follows:

$$Z_{O1} = \frac{1}{Y_{AI}+g_{ds1}+s\big(C_{d1}+C_L+C_{ds1}+C_{gd1}\big)} \parallel Z_{in2} \quad (8)$$

The term Z_{in2} will be addressed later within the CG-CS stage. The current gain for the input stage is expressed as:

$$\frac{I_{O1}}{I_{in1}} = \frac{Z_{TIA1}}{Z_{O1}} \quad (9)$$

The f_{-3dB} bandwidth of the proposed TIA topology is therefore worked out as:

$$f_{-3dB} = \frac{P}{2\pi C_{eq1}} \quad (10)$$

The combinational topology of CG-CS has the CS configuration with a gate that draws no current (at low frequencies), hence, a current gain of infinity (theoretically) can be exhibited.

The high input impedance of the CS core is in parallel with the CG input terminal which has far lower input impedance. Voltage headroom through the gate-to-source voltage of transistor M_{10} is easily overcome since node $in2$ carries the DC voltage from node O_1 and a fraction of the DC budget supply of 1V. The small-signal model of the CG-CS stage is shown in Fig. 5.

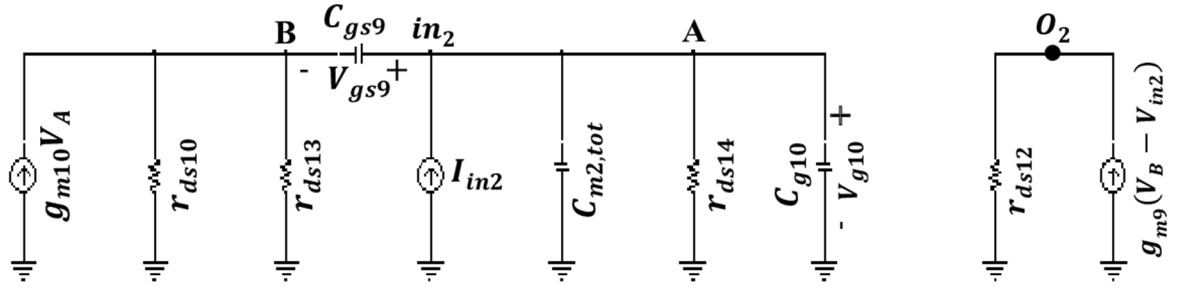

FIG. 5. Small-signal model of the CG-CS stage.

$$I_{in2} = V_{in2}(g_{m9} + g_{mb9} + g_{ds9} + g_{ds11} + C_{in2,tot}) - V_B(g_{m9} + sC_{gs9}) - V_{O2}(g_{ds9} + sC_{ds9}) \quad (11a)$$

$$0 = V_A\left(g_{ds14} + s\left(C_{d14} + C_{g10}\right)\right) - V_B sC_{gd10} - V_{in2} sC_{g10} \quad (11b)$$

$$0 = V_B\left(g_{ds13} + g_{ds10} + s\left(C_{d10} + C_{g9} + C_{d13}\right)\right) - V_A(g_{m10} - sC_{gd10}) - V_{O2} sC_{gd9} \quad (11c)$$

$$0 = V_{O2}(g_{ds12} + g_{ds9} + s(C_{d9} + C_{d12})) + V_B(g_{m9} - sC_{gd9}) - V_{in2}(g_{m9} + g_{mb9} + g_{ds9} + sC_{gd9}) \quad (11d)$$

where $C_{in2,tot} = C_{O1} + C_{s9} + C_{d11} + C_{g10}$ as $C_{O1} = C_{d1} + C_{d5}$. There is no actual gain from node $in2$ to node A, it is rather a transfer of impedance. However, for the sake of representation, the following formula is worked out based on Eq. (11b):

$$A_{in2A} = \frac{V_A}{V_{in2}} = \frac{sC_{g10}}{g_{ds14} + s(C_{d14} + C_{g10})} \quad (12)$$

Voltage gain from node A to node B is represented as:

$$A_{AB} = \frac{V_B}{V_A} = \frac{g_{m10}}{g_{ds13} + g_{ds10} + s(C_{d10} + C_{g9} + C_{d13})} \quad (13)$$

The voltage gain of the CG-CS stage is introduced as:

$$A_{v2} = \frac{g_{m9}(1 + |A_{in2A}A_{AB}|) + g_{mb9} + g_{ds9}}{g_{ds12} + g_{ds9} + s(C_{d9} + C_{d12})} \quad (14)$$

The input impedance of the CG-CS stage is manifested as follows which was indicated back in Eq. (8):

$$Z_{in2} = \frac{1}{Q + sC_{eq2}} \quad (15)$$

Whereas fractional Q is given as:

$$Q = g_{m9}(1 + |A_{in2A}A_{AB}|) + g_{mb9} + g_{ds9} + g_{ds11} - A_{v2}g_{ds9} \quad (16)$$

The equivalent input capacitance for the CG-CS stage is $C_{eq2} = C_{in2,tot} + |A_{in2A}A_{AB}|C_{gs9}$, while the CG-CS TIA gain is:

$$Z_{TIA2} = \frac{V_{O2}}{I_{in2}} = Z_{in2}A_{v2} \quad (17)$$

The overall TIA gain for the proposed topology is:

$$Z_{TIA} = \frac{I_{O1}}{I_{in1}} \times \frac{V_{O2}}{I_{in2}} \quad (18)$$

where $I_{O1} = I_{in2}$ in which a current gain of the input stage is multiplied by the TIA gain of the CG-CS stage as in the above equation.

3. Noise Analysis

The following equation is based upon an experimental common formula [16], however with a unique expression that describes the mean square channel thermal noise voltage (spectral density) at transistor M_1's drain:

$$\overline{V_{no,d1}^2} = 4kT\alpha g_{m1}(Z_{TIA1} - Z_{O1})^2 \quad (19)$$

where $\alpha = \gamma(g_{d0}/g_m)$, as γ is the channel thermal noise coefficient, and g_{d0} is the zero bias drain conductance. The drain of transistor M_2 mean square channel thermal noise voltage is:

$$\overline{V_{no,d2}^2} = 4kT\alpha g_{m2}\left(Z_{TIA1} - Z_X\frac{A_{v1}}{A_{M2}}\right)^2 \quad (20)$$

Here, $A_{v1}/A_{M2} = V_{O1}/V_X$, where Z_X is the impedance at node X. The mean square channel thermal noise voltage at the drain of transistor M_3 is:

$$\overline{V_{no,d3}^2} = 4kT\alpha g_{m3}\left(Z_{TIA1} - Z_Y \frac{A_{v1}}{A_{M2}A_{M3}}\right)^2 \quad (21)$$

Here, $A_{v1}/(A_{M2}A_{M3}) = V_{O1}/V_Y$, where Z_Y is the impedance at node Y. An update to the approach from prior literature [16] incorporates short channel effects [18] for the mean square induced gate noise voltage (spectral density) of transistor M_1. The expression for the mean square induced gate noise voltage is:

$$\overline{V_{no,g1}^2} = 4kT\delta \frac{(\omega C_{gs1})^2}{5g_{d01}}\left(Z_{TIA1} - Z_Y \frac{A_{v1}}{A_{M2}A_{M3}}\right)^2 \quad (22)$$

where δ is the gate noise coefficient. The shunt conductance (g_g) is redefined here as $\left[(\omega C_{gs1})^2/5g_{d01}\right]$. Previously, it was considered as $[(\omega C_O)^2/g_{d01}]$, where C_O represented the gate-oxide capacitance. The mean square induced gate noise voltages (for transistors M_2 and M_3) are:

$$\overline{V_{no,g2}^2} = 4kT\delta \frac{(\omega C_{gs2})^2}{5g_{d02}}(Z_{TIA1})^2 \quad (23)$$

$$\overline{V_{no,g3}^2} = 4kT\delta \frac{(\omega C_{gs3})^2}{5g_{d03}}\left(Z_X \frac{A_{v1}}{A_{M2}}\right)^2 \quad (24)$$

The common form of the overall gate and drain noise contribution is defined as [16]:

$$\overline{V_{no,Mx}^2} = \overline{V_{no,dx}^2} + \overline{V_{no,gx}^2} + 2|c|\sqrt{\overline{V_{no,dx}^2}.\overline{V_{no,gx}^2}} \quad (25)$$

where c is the cross-correlation coefficient (drain-to-gate noise). Transistor M_4 noise voltage contribution is defined in this work as:

$$\overline{V_{no,M4}^2} = 4kT(Z_{TIA1})^2 g_{ds4} \quad (26)$$

The noise voltage contribution of the PMOS current sources (M_5 and M_8), as well as transistors M_6 and M_7, is uniquely defined in this work as:

$$\overline{V_{no,r}^2} = 4kT\left(Z_O^2 Y_{AI} + Z_x^2 g_{ds6}\left(\frac{V_o}{V_x}\right)^2 + Z_y^2 g_{ds7}\left(\frac{A_{v1}}{A_{M2}A_{M3}}\right)^2\right) \quad (27)$$

The total noise contribution based on integrated mean square noise voltage (spectral density) is:

$$\overline{V_{no}^2} = \overline{V_{no,M1}^2} + \overline{V_{no,M2}^2} + \overline{V_{no,M3}^2} + \overline{V_{no,M4}^2} + \overline{V_{no,r}^2} \quad (28)$$

As a result, the input-referred noise current is given by the following common formula:

$$\overline{I_{in}^2} = \frac{\overline{V_{no}^2}}{(Z_{TIA1})^2} \quad (29)$$

4. Results

Channel length modifications using 45, 90, and 130 nm scales for the proposed TIA circuit topology (Fig. 3) are presented with corresponding TIA gain in Fig. 6(a). Ranging from 45, 90, and 130 nm scale, as the f_{-3dB} bandwidth is reduced, the TIA gain increases. Specifically, bandwidths of 1.68, 1.35, and 1.10 GHz correspond to 44.78, 46.39, and 47.94 dBΩ, respectively. Similar ohmic TIA gain behavior is manifested in Fig. 6(b). For the same bandwidths of 1.68, 1.35, and 1.10 GHz the respective ohmic gains are 173.434, 208.74, and 259.70 Ω, respectively.

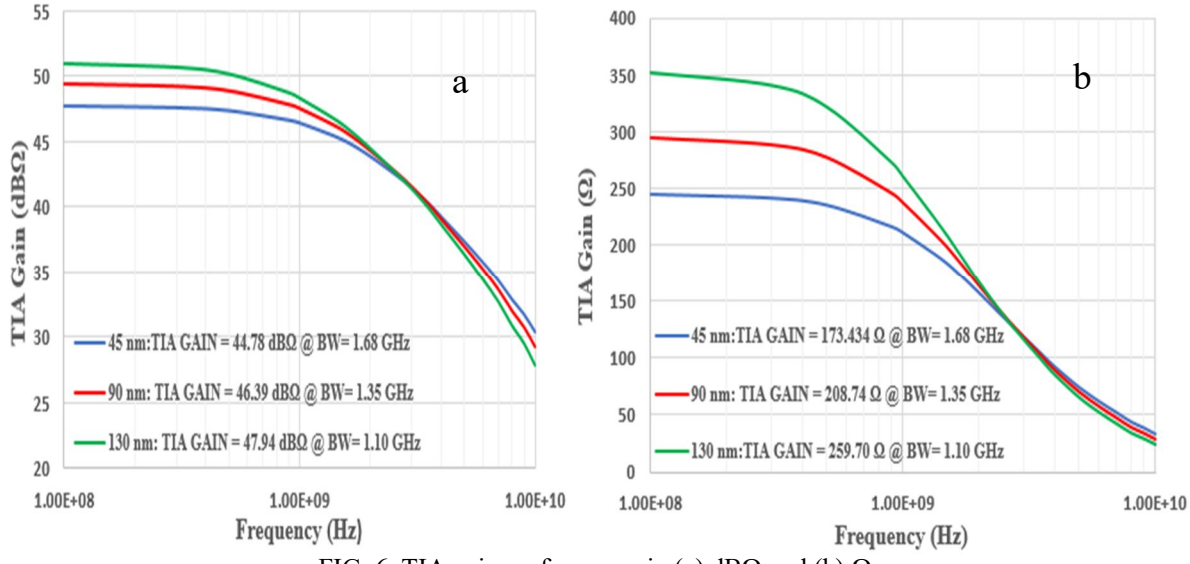

FIG. 6. TIA gain performance in (a) dBΩ and (b) Ω.

The reduction in bandwidth—1.68, 1.35, and 1.10 GHz—correlates directly with a rise in input impedance, as shown in Fig. 7, where the input impedance values are 230.93, 288.22, and 349.19 Ω for the channel lengths of 45, 90, and 130 nm, respectively. In contrast, the input-referred noise current (spectral density), shown in Fig. 8, decreases inversely to the input impedance. Specifically, the noise current reduces to 15.24 $pA/\sqrt{H_z}$, 10.77 $pA/\sqrt{H_z}$, and 9.40 $pA/\sqrt{H_z}$. This inverse relationship between input impedance and input-referred noise highlights a trade-off where increasing the channel length leads to a reduction in noise current, further impacting the bandwidth as a result.

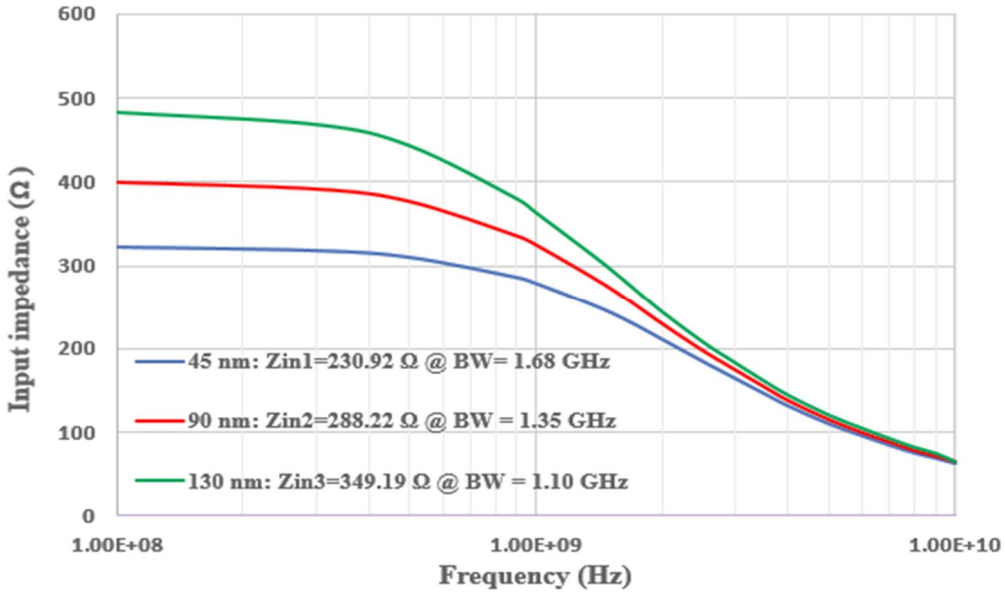

FIG. 7. Input impedance frequency dependence as per each channel length.

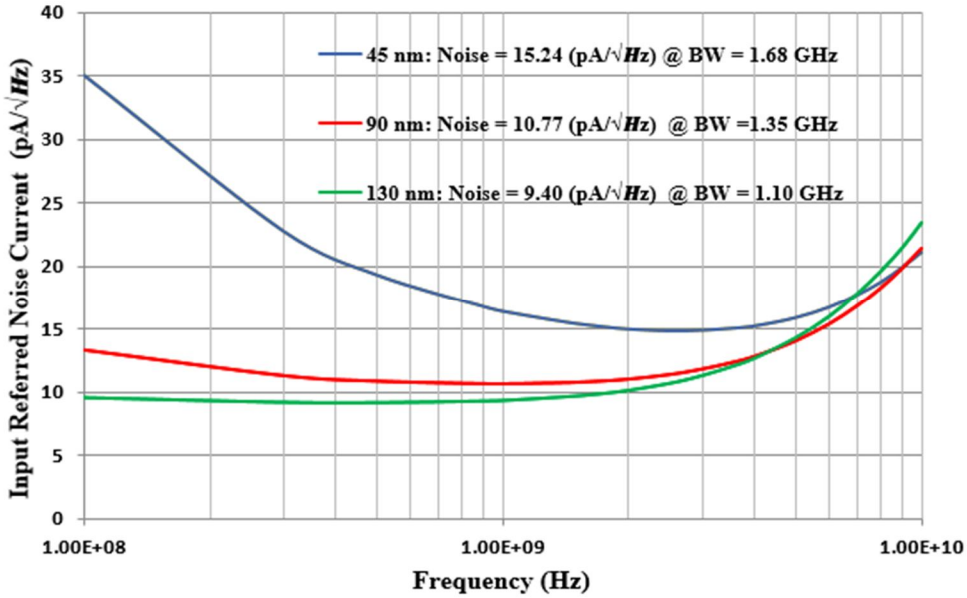

FIG. 8. Input referred noise current spectral density as per each channel length.

The total power consumption is confined to 0.621, 0.29, and 0.175 mW for the channel lengths of 45, 90, and 130 nm, respectively (Fig. 9). In addition, an individual transistor consumption is also shown. The most power-consuming transistors are M_6, $M_{12,}$ and M_{14}. The 45 nm scale consumes more than twice the power of the 90 nm scale and over three times the power of the 130 nm scale.

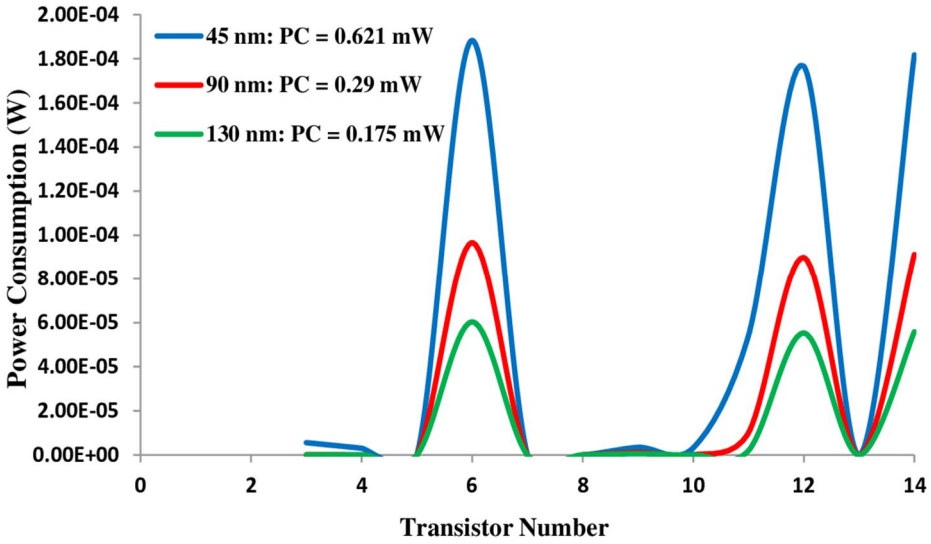

FIG. 9. Power consumption as per each transistor number for the channel length series (45, 90, and 130 nm).

The simulated active inductor impedance, based on extracted data, exhibits a frequency response that somewhat resembles the behavior of a spiral inductor. As shown in Fig. 10, an impedance divergence is observed in the 45 nm scale when compared to the 90 nm and 130 nm scales. This divergence arises from the onset of overlap between the depletion layers extending from the drain towards the source, an effect known as drain-induced barrier lowering (DIBL), which results from short-channel effects. To facilitate a clearer representation, a low frequency of 5 Hz is used.

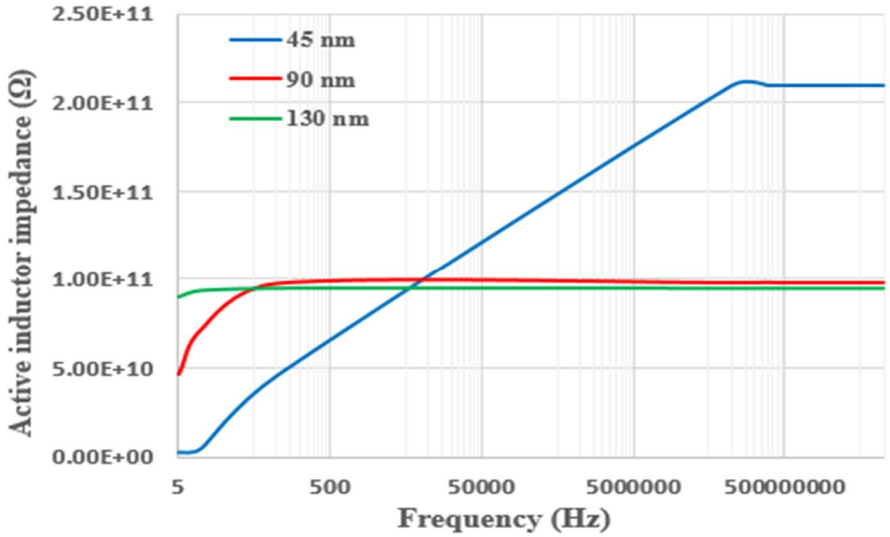

FIG. 10. Calculated active inductor impedance for the channel length series (45, 90, and 130 nm).

The eye diagram for the 45 nm TIA topology is presented in Fig. 11(a). The measure of jitter is around 0.07 ns which is the time variation of zero crossing, while the best time to sample is around 0.4 ns which is the decision point in which the most open part of the eye is equivalent to the best SNR. The signal-to-noise ratio at the sampling point is equivalent to 24.5 mV. The slope corresponds to a change in voltage swing of 15 mV versus a change of 0.09 ns. This slope is relatively small which indicates the sensitivity to timing error. As in the 90 nm scale for the same TIA topology, shown in Fig. 11(b), the measure of jitter is around 0.04 ns, while the best time to sample is around 0.45 ns. The signal-to-noise ratio at the sampling point is equivalent to 32 mV. The slope corresponds to a change in voltage swing of 10 mV versus a change of around 0.04 ns. Regarding the 130 nm scale for the same TIA topology, shown in Fig. 11(c), the

measure of jitter is around 0.04 ns, while the best time to sample is around 0.47 ns. The signal-to-noise ratio at the sampling point is equivalent to 36 mV. The slope corresponds to a change in voltage swing of 8 mV versus a change of around 0.03 ns. The bandwidth series (1.68, 1.35, and 1.10 GHz) and the vertical and horizontal eye openings shown in Fig. 11 indicate very limited intersymbol interference (ISI) in random data transmission. Although the bandwidth is lower at the 90 nm and 130 nm scales, corresponding to 1.35 GHz and 1.10 GHz respectively, a 1.5 Gb/s input bit sequence was applied for comparative performance purposes.

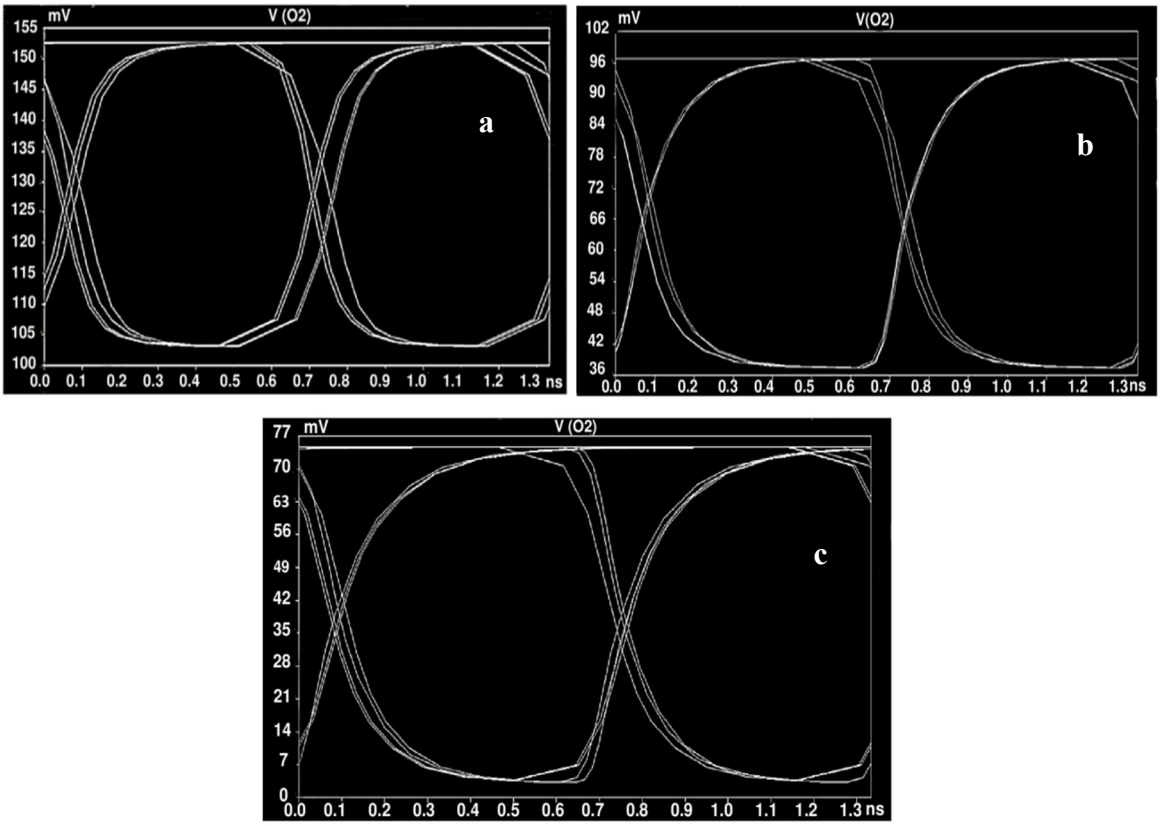

FIG. 11. Eye diagram using bit sequencing at 1.5 Gb/s for : (a) 45 nm scale, (b) 90 nm scale, and (c) 130 nm scale.

For the 45 nm scale, Table 1 illustrates a clear trade-off in TIA gain, bandwidth, and input-referred noise, showing balanced performance. In related literature, the lowest reported power consumption is 0.01 mW [3], though the supply voltage is unspecified. When comparing the power consumption of 0.621 mW achieved in this study with other references [4,19], it becomes evident that, while the gain level of 44.78 dBΩ in this work is moderately lower, the achieved power efficiency offers a competitive advantage in application-specific contexts, particularly given the f_{-3dB} bandwidth of 1.68 GHz.

TABLE 1. Comparative performance for 45 nm scale in relation to other literature.

Ref.	[4]	[19]	[3]	This Work
Year	2010	2018	2022	2023
CMOS Technology	45 nm	45 nm	45 nm	45 nm
TIA Gain (dBΩ)	55	74.4	140	44.78
Bandwidth	30	23	10 MHz	1.68 GHz
Input Referred Noise ($pA/\sqrt{Hz}$)	20.47	12	4.6	15.24
Power Consumption (mW)	9	36.6	0.01	0.621
DC Supply Voltage (V)	1	1	-	1

Table 2 provides a balanced comparison between this work and the cited literature [20-21]. There is an indirect relationship between power consumption and bandwidth, which highlights the trade-off between bandwidth and TIA gain. The power consumption level of 0.29 mW in this work is more than three times lower than that reported in the comparative literature [20, 21]. However, the f_{-3d} bandwidth in the comparative studies is over five times higher, with results for TIA gain and input-referred noise being closer, given that a 1.2V DC supply voltage is applied in that literature [20]. Due to the mentioned trade-off relationships, other studies [22] appear to focus on different applications other than power consumption reduction as a key advantage. The same approach is followed in Table 3 in which there are some divergent results between this work and the cited literature [7, 23] in terms of TIA gain. Given the compromise of achieving a low power consumption of just 0.175 mW in this work, this divergence is expected. However, it is important to note that a 1.5 V DC supply budget is applied in the referenced studies [7, 23], compared to the 1V used in the proposed TIA topology. The high power consumption reported in the cited literature [24] is associated with high input-referred noise, which represents a significant difference from this work, especially since no specific DC supply voltage is indicated in that context.

TABLE 2. Comparative performance for 90 nm scale in relation to other literature.

Ref	[20]	[21]	[22]	This Work
Year	2019	2020	2021	2023
CMOS Technology	90 nm	90 nm	90 nm	90 nm
TIA Gain (dBΩ)	50.5	41	39.8	46.39
Bandwidth (GHz)	7.3	6.5	24.8	1.35
Input Referred Noise ($pA/\sqrt{H_Z}$)	13.7	33.4	50	10.77
Power Consumption (mW)	1	1.67	11.6	0.29
DC Supply Voltage (V)	1.2	1	-	1

TABLE 3. Comparative performance with other literature for 130 nm scale.

Ref	[7]	[23]	[24]	This Work
Year	2015	2019	2021	2023
CMOS Technology	130 nm	130 nm	130 nm	130 nm
TIA Gain (dBΩ)	52.4	59.885	66	47.94
Bandwidth (GHz)	8.2	6.9	40	1.10
Input Referred Noise ($pA/\sqrt{H_Z}$)	1.94 μArms	7.925	9.4	9.40
Power Consumption (mW)	3.6	0.872	142	0.175
DC Supply Voltage (V)	1.5	1.5	-	1

5. Discussion

In the input stage shown in Fig. 3, the active inductor is configured using two PMOS structures (transistors M_5 and M_8). In this configuration, the conditions of having a single MOSFET operating in saturation as a current source do not apply, yet the active inductor can still maintain a stable voltage at node O_1 given the fact that channel length modulation parameter $\lambda \neq 0$. The drain terminal of transistor M_5 can draw a DC current and present high impedance. The significant impedance of the active inductor behaves like an ideal current source, exhibiting nearly infinite small-signal resistance.

Theoretically, the highest possible voltage gain for transistor M_1 is given by $(-g_{m1}r_{O1})$. However, the output node resistance of transistor M_1 is determined by the parallel combination of its own output resistance (represented by the active inductor impedance at low frequencies and the input resistance of the second CG-CS stage. A key advantage of having the active inductor current source is its ability to alleviate the trade-off between voltage gain and the voltage headroom $(V_{GS1} - V_{th})$ so far as transistor M_1 is concerned.

The degeneration output resistance of transistor M_4 sustains a fraction of the input voltage at node $in1$. From the perspective of the

CG configuration, the photodiode input signal is delivered as a current, causing the voltage at node $in1$ to increase by ΔV_{in1}. Consequently, the gate-to-source voltage of transistor M_1 decreases by similar amount, leading to a reduction in drain current by $g_{m1}\Delta V_{in1}$ and consequently, an increase in output voltage at node O_1. The input pole magnitude described in Eq. (1) is maximized within the CG structure by maximizing g_{m1}, which can be achieved by increasing the drain current. This leads to higher gate-to-source and minimum allowable drain-to-source voltages for transistors M_1 and M_4, respectively, along with an increased voltage drop across the active inductor impedance Z_{AI} at the DC level. The 1V supply voltage is sufficient to support these voltage headroom requirements. Interestingly, Z_{AI} is extremely high across the bandwidth series (1.68, 1.35, and 1.10 GHz), and even at lower frequencies as shown in Fig. 10. This high level of Z_{AI} contributes to the suppression of input-referred noise and prevents the magnitude of Z_{TIA1} from falling. The biasing of transistor M_4 is set high enough to allow a reasonably elevated drain-to-source voltage, thereby reducing noise and drain capacitance. Despite the challenging constraints, a broadband topology with a reasonably high transimpedance gain was achievable in this work, even with a low supply voltage of 1V.

The CG drawbacks were overcome since transistor M_1 not only serves as active feedback but is also in a CG configuration. The first CG drawback is that the noise scales in a direct way with $C_{in,tot1}$ and frequency; as $sC_{in,tot1}$ increases, a significant fraction of the noise contributed by transistor M_1 does not circulate inside it but instead flows from the output node O_1. The second drawback, which is often expected, is that the noise contributed to the input by the DC component of Z_{AI} rises as $|sC_{in,tot1}|$ becomes comparable to g_{m1}. This is typically observed since the TIA gain tends to decrease as the signal frequency approaches the input pole.

Within the CG-CS stage, the low input impedance of the CG core (ignoring the high CS input impedance) enables a wider bandwidth of the CG-CS topology, accommodating the time constant of the output node O_1 from the input feedforward stage. The combined CG-CS output impedance is determined by how low is the output conductance of transistors M_{12} and M_{13}. Given the high output resistances of transistors M_9 and M_{10}, it was not possible to neglect channel length modulation. The CG stage on its own suffers from a trade-off between gain and overdrive voltage, the drain resistance of transistor M_9 is high enough to achieve a considerable voltage gain.

With regard to channel length modification effects on input impedance and TIA gain, the upward direction in channel lengths (45, 90, and 130 nm) for the identical proposed TIA topology leads to increases in both TIA gain and input impedance as illustrated in Fig. 6 and Fig. 7. According to Eq. (6), the increase in input impedance (with increasing channel length) is attributed to the decrease in g_{m1} (transconductance of transistor M_1). This decrease in g_{m1} occurs due to the narrower variation in gate-to-source voltage and, subsequently, a reduced variation in drain current for transistor M_1 as channel length increases. Similarly, the decrease in the transconductance parameter g_{m2} for the pass transistor M_2 affects input impedance in the same manner as observed in transistor M_1. Subsequently, an increase in input impedance contributes to the increase in TIA gain of the input stage (Z_{TIA1}) according to Eq. (5). The term $|A_{M2}A_{M2}|$ plays an important role in determining the input stage voltage gain (A_{v1}), which has an inverse relation with input impedance as described in Eq. (5). For a single transistor, there is a proportional relationship between channel length L and voltage gain A_v, expressed as $|A_v| \propto \sqrt{2\mu_n C_{OX} WL/I_D}$ [17]. This relationship remains true when generalized to the proposed circuit topology. Therefore, a higher voltage gain means a higher TIA gain across the channel length series (45, 90, and 130 nm).

Regarding the effects of channel length modification on bandwidth and input-referred noise, the increase in input impedance associated with the channel length series results in reduced bandwidth, lower input-referred noise, and lower power consumption. To be more precise, the DC input resistance is given by $1/P$ according to Eq. (6), hence, the f_{-3dB} bandwidth is governed by this resistance alongside the equivalent input parasitic capacitance C_{eq1}. Therefore, the rise in input impedance shown in Fig. 7 across the channel length series (45, 90, and 130 nm) leads to a reduction in bandwidth (1.68, 1.35, and 1.10 GHz). From the perspective of input-referred

noise shown in Fig. 8, the rise in input impedance along the channel length series causes an increase in Z_{TIA1} gain according to Eq. (5). Given the square Z_{TIA1} term in Eq. (29), this inevitably leads to a reduction in input-referred noise current along the series. The inverse relationship between $\overline{I_{in}^2}$ and $(Z_{TIA1})^2$ as in Eq. (29) may not be straightforward, since the total integrated mean square noise voltage spectral density contribution $\overline{V_{no}^2}$ also contains $(Z_{TIA1})^2$ in various terms. However, the impact of $\overline{V_{no}^2}$ is minimized. For instance, in Eq. (19), the term $(Z_{TIA1} - Z_{O1})^2$ clearly indicates the subtraction of the input stage output impedance Z_{O1}, especially since $g_{ds1} \gg Y_{AI}$ as in Eq. (8), considering that the active inductor impedance Z_{AI} is extremely high at the bandwidth series (1.68, 1.35, and 1.10 GHz) shown in Fig. 10.

In terms of the effects of channel length modification on power consumption reduction, the upward trend in channel length correlates with the output resistance of each individual transistor, since $r_O = (\lambda I_D)^{-1}$. Given that $\lambda \propto L^{-1}$ and considering the channel length series (45, 90, and 130 nm), a new form of channel length modulation arises for the proposed TIA circuit topology. The series power consumption (0.621, 0.29, and 0.175 mW) shown in Fig. 9 corresponds to the aforementioned channel length series, which is attributed to the rise in output resistance of each transistor. PMOS current sources, such as transistors M_6, M_{12} and M_{14}, exhibit higher power consumption compared to other transistors. For transistor M_6, an additional drain current is drawn due to the biasing of transistor M_2 in a degenerative configuration, where its source is connected to the drain of the biasing transistor M_4, resulting in an extra drain current. Transistor M_{12} also has a degeneration path through the drain of transistor M_{11}, and similarly for transistor M_{14}. Based on the above argument, it is valid to say that the 45 nm scale indicates the highest power consumption, although it is still far lower than values reported in other literature. It is also possible that there was an overlap in the depletion regions between the drain and source in the 45 nm scale, which could have led to higher output resistance due to short-channel effects, specifically drain-induced barrier lowering (DIBL).

In the comparative performance analysis tables, an important concept emerges regarding the trade-offs among TIA gain, bandwidth, and input-referred noise. This trade-off is evident in the 45 nm scale literature presented in Table 1, as well as in the rest of the channel length series (45, 90, and 130 nm) for the proposed TIA topology shown in Fig. 3. For application-specific criteria, power consumption reduction does not exactly and fully follow the trends observed in the comparative literature presented in Tables 1, 2, and 3, as the channel length increases from 45, 90, and 130 nm. This discrepancy is due to the selective nature of certain applications that may relax the original trade-offs in TIA gain, bandwidth, and input-referred noise. Nonetheless, the general principle that power consumption reduces with increasing channel length (for similar or different topologies) remains valid in most cases.

Conclusion

A proposed TIA was designed, analyzed, and simulated with channel length modification. It was found that a trade-off between gain, bandwidth, and input-referred noise current can still apply as the channel length is increased from 45, 90, and 130 nm. In addition, power consumption reduction occurred with the upward modification of channel length for the same topology.

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