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ARTICLE

A Low-Power 45 nm CMOS Transimpedance Amplifier with Active Inductor Feedback for Fiber-Optic Applications

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Abstract: In this paper, a transimpedance amplifier (TIA) is introduced to obtain low power consumption with moderately high gain. The proposed TIA consists of two parts: in the first stage, a regulated cascade transimpedance amplifier (RGC TIA) input stage with active inductor local feedback is utilized for current gain enhancement, while a second stage is designed for TIA gain. The proposed TIA circuit is implemented in a 45 nm CMOS process technology. Simulation results show that the proposed TIA achieves a power consumption of 0.975 mW, while the TIA gain is increased up to 62.2 dBΩ at 1 GHz of f_{-3dB} bandwidth. The conventional trade-off between gain and power consumption is relaxed, which represents the key finding of this work, while maintaining an input-referred noise current spectral density of 28pA/√Hz. The reported low power consumption was achieved at a 1V budget DC supply.

Keywords: Optical preamplifier, Fiber optics, RGC transimpedance, TIA gain.

PACs: 85.40.-e, 07.50. Ek, 84.30.-r

1. Introduction

Fiber-optic communications have attracted demand in the field of high-speed data transmission due to their high bandwidth features with low power consumption. An RGC TIA input topology employs a positive amplifier with an inductor that controls the circuit input impedance and isolates large input parasitic capacitance [1]. A modified RGC TIA followed by a closed-loop post amplifier was proposed for 10 Gb/s applications to reduce power consumption while extending bandwidth considerably [2]. A G_m/I_D methodology was proposed for the design of an RGC TIA, where the sizing of transistors was defined using this particular methodology [3]. An RGC modification in TIA followed by closed-loop gain stage with an added voltage level shift to the RGC booster, was considered [4]. A modified MOS-based impedance converter combined with an RGC TIA was proposed to achieve low power consumption and high bandwidth [5]. An RGC structure was cascaded with a shunt-feedback TIA, in which an inductor was added between the two topologies, forming a π-type matching network [6]. A shunt feedback TIA that employs a three-stage nested Miller compensated (NMC)-based design was demonstrated [7]. A double-cascade TIA with negative shunt-shunt feedback and inductive peaking technique was utilized [8]. A bandwidth enhancement technique (based upon π peaking network) for a resistive shunt-feedback TIA was employed [9]. A negative Miller capacitance approach was proposed for extending the bandwidth of shunt feedback TIA [10]. An early implementation of a shunt-shunt feedback TIA using 0.18 μm CMOS technology was reported [11]. Combined concepts of input-stage feedforward followed by a current mirror stage with local active-inductor feedback were reported using 45 nm CMOS technology [12].

This work aims to achieve low power consumption and high TIA gain, while maintaining a relatively low input-referred noise current spectral density.

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1.1 RGC TIA Input Stage

The low-input resistance of common-gate (CG) topologies is always attractive for optimizing the design of TIAs. It is shown in Fig. 1a that in the CG structure, the input resistance can be illustrated as given [2]:

$$R_{in} = \frac{R_S}{1+R_S g_{m1}} \quad (1)$$

Indicating that g_{m1}, it is the transconductance parameter of the transistor M_1 as in Eq. (1), the width of M_1 has a crucial impact on lowering the input resistance of a CG stage. In addition, in the RGC topology manifested in Fig. 1b, the transconductance of M_1 can be increased by a factor of $(1 + g_{m2}R_B)$ for which transistor M_2 works as a booster amplifier stage. The input resistance of the RGC structure can be written as in the following expression, where channel length modulation is neglected for the sake of argument:

$$R_{in} = \frac{R_S}{1+R_S g_{m1}(1+g_{m2}R_B)} \quad (2)$$

The input resistance can be lowered if the booster amplifier gain $g_{m2}R_B$ is raised. When a cascode transistor is added, a further isolation of the input capacitance is possible in order to achieve a high-speed TIA. Since the RGCs cannot provide sufficient gain at low supply voltage, a gain stage can be added, which may consume low power [13].

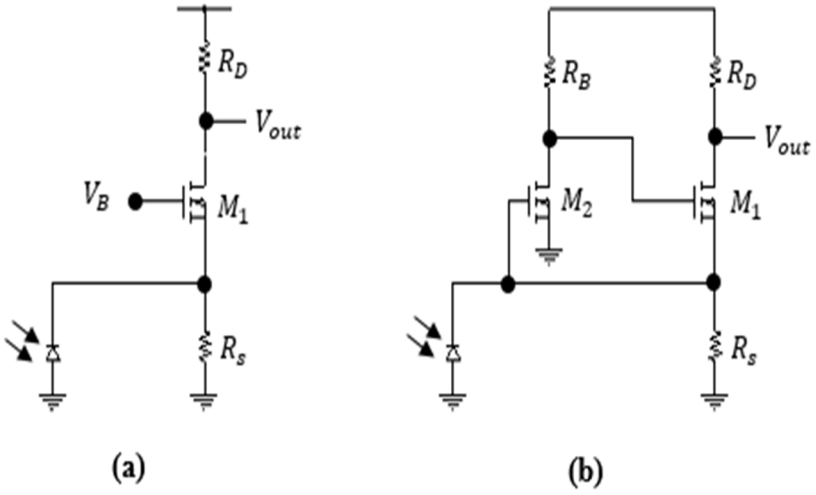

FIG. 1. (a) CG TIA topology (b) Conventional RGC TIA topology.

2. Proposed TIA Topology

In Fig. 2, an input stage with active inductor feedback is introduced. It consists of a CG structure within the transistor M_1 configuration that initiates a voltage gain from node $in1$ to node $O1$. This voltage gain is combined with the gain from node Y to node $O1$ through a CS dual role of transistor M_1. The current gain path of transistor M_1 is stabilized by the triode-configured transistor M_3. The CS configuration of transistor M_2 raises the DC voltage level from node X to node Y in order to accommodate enough voltage headroom for transistor M_1. The active inductor feedback is constructed with PMOS transistors M_{12} and M_{13} with identical aspect ratio (W/L). The output node $O1$ is an input for the second stage at the gate of transistor M_5 in CS configuration. Effectively, the gate resistance R_{G5} of transistor M_5 (being extremely high) is in parallel with the low drain resistance r_{f2} of transistor M_7. This transistor is in an active feedback loop involving the source follower transistor M_4. The equivalent resistance $r_{f2} \| r_{g5}$ ($\approx r_{f2}$ where r_{g5} is too high) enables fractional feedback from the node $O2$ (*i.e.,* gate of transistor M_4) *via* transistor M_7. Transistor M_4 works as a level-shift component in which any rise in the output voltage at node $O2$ tends to increase the gate-to-source voltage of M_4, hence raising its drain current and eventually its output voltage. Notably, the equivalent resistance ($\approx r_{f2}$) contributes to satisfying the condition $V_{GS5} > V_{TH5}$ for transistor M_5, boosting its transconductance parameter g_{m5} to a higher level, enhancing the voltage gain at the node $O2$ via boosted CG structure of transistor M_6.

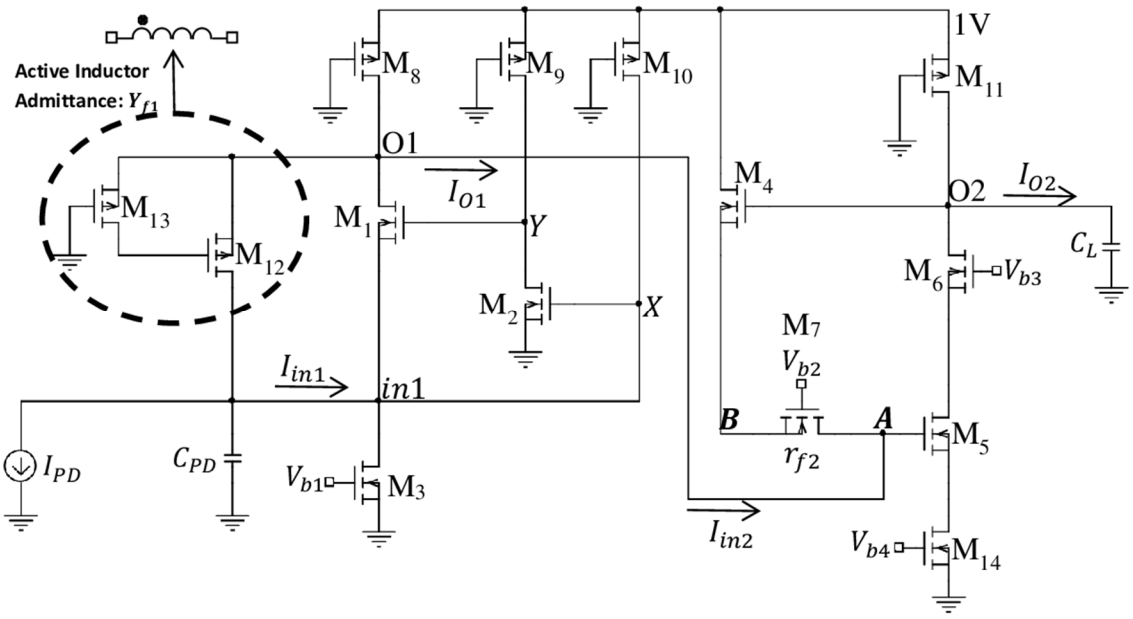

FIG. 2. Proposed TIA topology.

In brief, the signal path in Fig. 2 is split at the input node $in1$. The CG role of transistor M_1 receives part of the signal, while the other part is within the role of CS transistor M_2, which draws no current at its gate; however, its V_{GS2} enables the drain current path to conduct. The joint voltage gain of transistor M_1 and M_2 is identified at node Y, then it is finally amplified at the output node $O1$ for the input stage to form a current gain primary stage. In the subsequent stage, node A is essentially jointed with a node $O1$. The drain current conduction of transistor M5 depends on the signal path in the form of a voltage drop at the node A. A significant voltage gain is formed at the node $O2$ which is fed back through a common drain role of transistor M_4 with a fractional signal path ending up at the source of feedback transistor M_7 with CG role at node B, hence amplifying the signal with a voltage drop at the node A, thereby continuing the amplification process.

2.1 Input Stage

The small signal model of the input stage is envisaged in Fig. 3. The transfer of impedance from node $in1$ to node X can initiate driving capability for transistor M_2. However, the voltage drops on the node $in1$ controls the voltage difference with the output node $O1$ *via* the component for low admittance Y_{f1} (active inductor feedback). Actual conduction of transistor M_1 is enabled by the voltage difference between a node $in1$ and node Y.

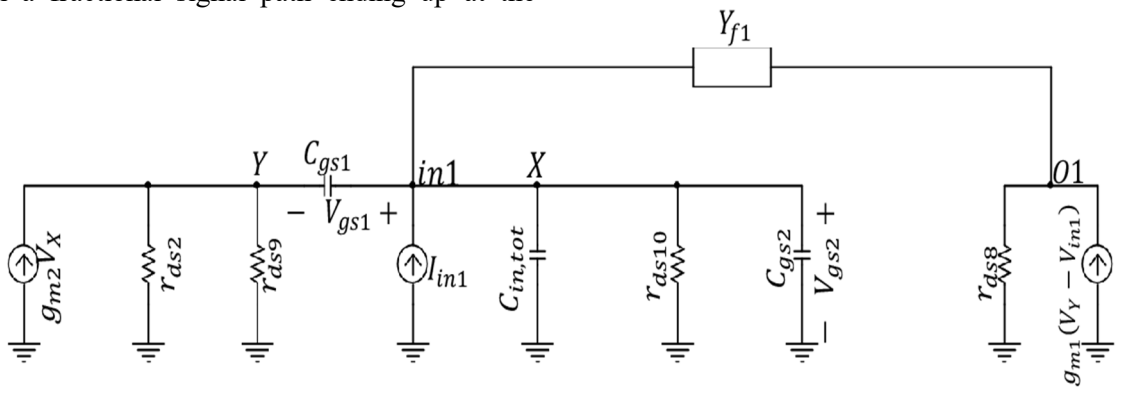

FIG. 3. Small signal equivalent circuit model of the input stage using T-model transistor.

Based on the above small signal model, the following Kirchhoff Current Law (KCL) equations are summed as follows:

$$I_{in1} = V_{in1}\left(g_{m1} + g_{mb1} + g_{ds1} + g_{ds3} + sC_{in1,tot}\right) - V_Y\left(g_{m1} + sC_{gs1}\right) - V_{O1}\left(g_{ds1} + sC_{ds1} + Y_f\right) \quad (3)$$

$$0 = V_X\left(g_{ds10} + s\left(C_{d10} + C_{g2}\right)\right) - V_Y sC_{gd2} - V_{in1} sC_{gs2} \quad (4)$$

$$0 = V_Y\left(g_{ds9} + g_{ds2} + s\left(C_{d2} + C_{g1} + C_{d9}\right)\right) - V_X\left(g_{m2} - sC_{gd2}\right) \quad (5)$$

$$0 = V_{O1}\left(g_{ds8} + g_{ds1} + Y_f + s(C_{d1} + C_{d8})\right) - V_Y\left(g_{m1} - sC_{gd1}\right) - V_{in1}(g_{m1} + g_{mb1} + g_{ds1} + sC_{ds1}) \quad (6)$$

Strictly, a transfer of impedance from node $in1$ to node X with near unity voltage gain as given:

$$A_2 = \frac{V_X}{V_{in1}} = \frac{sC_{gs2}}{g_{ds10} + s\left(C_{d10} + C_{g2}\right)} \quad (7)$$

The voltage gain from the node X to node Y raises the DC voltage level at the node Y and is represented as:

$$A_3 = \frac{V_Y}{V_X} = \frac{g_{m2}}{g_{ds9} + g_{ds2} + s\left(C_{d2} + C_{g1} + C_{d5}\right)} \quad (8)$$

The input stage voltage gain is extended by a factor of $(1 + |A_2A_3|)$ with low feedback admittance Y_{f1} and is worked out as:

$$A = \frac{g_{m1}(1 + |A_2A_3|)}{g_{ds8} + g_{ds1} + Y_{f1} + s(C_{d1} + C_{d8})} = A_1(1 + |A_2A_3|) \quad (9)$$

The voltage gain of transistor M_1 is characterized as A_1, whereas the active inductor feedback impedance Z_{f1}, it is an inversion of the feedback admittance Y_{f1} as follows, based on the general equation [14]:

$$Z_{f1} = \frac{r_{ds13}C_{gs12}s + 1}{g_{m12} + C_{gs12}s} \quad (10)$$

The input impedance for the input stage heavily depends upon the extended factor of $g_{m1}(1 + |A_2A_3|)$, given as follows:

$$Z_{in1} = \frac{1}{P + sC_{eq1}} \quad (11)$$

As

$$P = g_{m1}(1 + |A_2A_3|) + g_{ds3} - A\left(g_{ds1} + Y_{f1}\right) \quad (12)$$

$$C_{eq1} = \left(C_{in1,tot} + A_2A_3C_{gs1}\right) \quad (13)$$

Whereas the DC input resistance (R_{in1}) is deduced as $1/P$, therefore the f_{-3dB} bandwidth is worked out as:

$$f_{-3dB} = \frac{1}{2\pi}\frac{P}{C_{eq1}} \quad (14)$$

The finite output impedance of the input stage is configured so that it delivers optimal current gain that contributes to the better driving capability of the subsequent stage. It is worth noting that the parasitic time constant of the output node $O1$ is governed by N as follows where $r_{g5} \gg r_{f2}$:

$$Z_{O1} = \frac{r_{ds8}(r_{f2} \| r_{g5})}{M + sN} \quad (15)$$

$$M = \left(r_{f2} \| r_{g5}\right)\left[Y_{f1}r_{ds8} + 1\right] + r_{ds8}$$

$$N = \left(C_{d1} + C_{d8} + C_{g5}\right)\left(r_{f2} \| r_{g5}\right)r_{ds8}$$

The input stage TIA gain is defined in terms of input impedance and voltage gain as follows:

$$Z_{TIA1} = Z_{in1}A \quad (16)$$

Whereas the current gain formula is worked out as follows:

$$\frac{I_{O1}}{I_{in1}} = \frac{Z_{TIA1}}{Z_{O1}} \quad (17)$$

2.2 Second Stage

The small signal model of the subsequent stage is represented in Fig. 4. The voltage drop between nodes A and B generates a fractional feedback drain current through a resistor r_{f2}. The level-shifting source follower M_4 is virtually grounded, and the current signal $g_{m4}V_{gs4}$ flows into node B. The voltage across the parasitic capacitance Cgs4C, connected between nodes B and O2, is equivalent to Vgs4.

Based on the above small-signal model, the KCL equations governing the nodal currents are expressed as follows:

$$-I_{in2} + V_A sC_{gs5} + \frac{(V_A - V_B)}{r_{f2}} = 0 \quad (18)$$

$$\frac{V_{O2}}{r_{ds11}} + g_{m5}V_A + (V_{O2} - V_B)sC_{gs4} = 0 \quad (19)$$

$$-g_{m4}(V_{O2} - V_B) - (V_{O2} - V_B)sC_{gs4} - \frac{(V_A - V_B)}{r_{f2}} = 0 \quad (20)$$

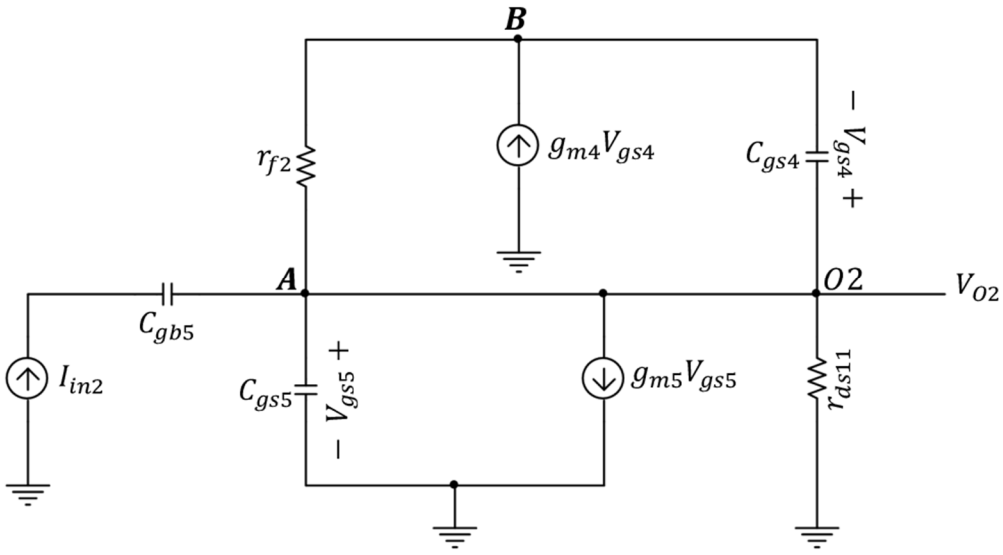

FIG. 4. Small-signal equivalent circuit of the proposed subsequent stage.

The TIA gain Z_{TIA2} of the proposed subsequent stage is therefore given as:

$$Z_{TIA2} = \frac{V_{O2}}{I_{in2}} = \frac{s^2a+sb+c}{s^4A+s^3B+s^2C+D} \quad (21)$$

where,

$$a = r_{f2}\left(C_{gs4}r_{ds11}C_{gs5} + C_{gs4}C_{gs5}r_{f2}\right)$$

$$b = \left(C_{gs4}r_{ds11} + r_{f2}\left(g_{m4}C_{gs5}r_{f2} + C_{gs4} + C_{gs5}\right)\right)$$

$$c = -g_{m5}g_{m4}r_{f2}$$

$$A = \left(C_{gs4}\right)^2 r_{ds11}\left(C_{gs5}\right)^2\left(r_{f2}\right)^2$$

$$B = C_{gs4}r_{ds11}C_{gs5}r_{f2}\left(C_{gs5}r_{f2}g_{m4} + C_{gs4}\right)$$

$$C = C_{gs4}(r_{ds11}g_{m4} - g_{m5} - 1) - C_{gs5}\left(g_{m5}g_{m4} - g_{m4}r_{f2} - 1\right)$$

$$D = -g_{m4}\left(g_{m5} + r_{f2}\right)$$

As a result, the overall TIA gain is introduced as:

$$Z_{TIA} = \frac{I_{O1}}{I_{in1}} \times \frac{V_{O2}}{I_{in2}} \quad (22)$$

Given that $I_{O1} = I_{in2}$, the overall TIA gain is expressed in terms of Eqs. (17) and (21).

3. Noise Analysis

Within CMOS transistors, operating in the frequencies of interest to this research, there is a potential fluctuation in a random pattern inside the channel which causes a form of channel noise. Through gate-oxide capacitance, the channel noise is permitted to the gate terminal, resulting in gate noise being induced [15]. The Van der Zeil model suggests the following formulas regarding the mean square drain current noise and the mean square induced gate-noise contribution, respectively [16].

$$\overline{I_d^2} = 4kT\alpha g_m \quad (23)$$

$$\overline{I_g^2} = 4kT\delta g_g \quad (24)$$

As $= \gamma\, g_{d0}/g_m$, where γ and δ denote the channel thermal noise coefficient and gate noise coefficients, respectively. The shunt conductance g_g is expressed as $\left(\omega C_{gs}\right)^2/5g_{d0}$ [17]. The term g_{d0} denotes the zero-bias drain conductance. In a CG configuration, the transistor source terminal acts as the signal node. Therefore, channel noise is injected through the gate and drain terminals, which are fully correlated. The mean-square spectral density of the channel thermal noise voltage contributed by the drains of transistors M_1 and M_2 can be expressed as:

$$\overline{V_{no,d1}^2} = 4kT\alpha g_{m1}(Z_{TIA1} - Z_{O1})^2 \quad (25)$$

$$\overline{V_{no,d2}^2} = 4kT\alpha g_{m1}(Z_Y A_{YO1})^2 \quad (26)$$

where A_{YO1} denotes the voltage gain from node Y to node $O1$, while Z_Y represents the net nodal impedance at node Y.

$$A_{YO1} = \frac{A_{v1}\left(g_{ds8}+g_{ds1}+s(C_{d1}+C_{d8})\right) - g_{m1} - g_{mb1} - g_{ds1}}{g_{m1}A_{v1}} \quad (27)$$

$$Z_Y = \frac{r_{ds9}r_{ds2}}{r_{ds2}+r_{ds9}+sC_{gs1}r_{ds9}r_{ds2}} \quad (28)$$

The mean-square spectral densities of the induced gate noise voltages generated by transistors M_1 and M_2 are given by:

$$\overline{V_{no,g1}^2} = 4kT\delta\frac{(\omega C_{gs1})^2}{5g_{d01}}(Z_{TIA1} - Z_Y A_{YO1})^2 \quad (29)$$

$$\overline{V_{no,g2}^2} = 4kT\delta\frac{(\omega C_{gs2})^2}{5g_{d02}}(Z_X A_{XO1})^2 \quad (30)$$

where g_d0x is the zero-bias drain conductance of transistor M_x. The voltage gain from node X to node $O1$ is expressed as A_{XO1}, while Z_X is the nodal impedance at node X.

$$A_{XO1} = \frac{A_2 A_Z(g_{m1} - sC_{gd1}) + g_{m1} + g_{mb1} + g_{ds1}}{A_Z\left(g_{ds8} + g_{ds1} + Y_{f1} + s(C_{d1} + C_{d8})\right)} \quad (31)$$

$$Z_X = \frac{r_{ds10}}{1 + sr_{ds10}(C_{gs2} + C_{in1,tot})} \quad (32)$$

The summation of the mean-square of the drain and gate induced noise voltages for M_1 and M_2 can be calculated as:

$$\overline{V_{no,Mx}^2} = \overline{V_{no,dx}^2} + \overline{V_{no,gx}^2} + 2|c|\sqrt{\overline{V_{no,dx}^2}.\overline{V_{no,gx}^2}} \quad (33)$$

The noise contribution of the current source M_3 is:

$$\overline{V_{no,M3}^2} = 4kT\frac{Z_{TIA}^2}{r_{o3}} \quad (34)$$

where r_{o3} is the equivalent drain to source resistance of M_3. The noise contribution of equivalent load resistance is shown as:

$$\overline{V_{no,r}^2} = 4kT\left(\frac{Z_{O1}}{r_{o1}} + \frac{Z_Y^2}{r_{o2}}A_{YO1}^2\right) \quad (35)$$

The output of the TIA carries the total noise, summed as:

$$\overline{V_{no}^2} = \overline{V_{no,M1}^2} + \overline{V_{nm,M2}^2} + \overline{V_{no,M3}^2} + \overline{V_{no,r}^2} \quad (36)$$

Therefore, the total input-referred noise current spectral density is expressed as:

$$\overline{I_{in}^2} = \frac{\overline{V_{no}^2}}{Z_{TIA}^2} \quad (37)$$

4. Results

The simulated TIA gain shown in Fig. 5 corresponds to 62.2 dBΩ at f_{-3dB} bandwidth of 1 GHz. The low-pass frequency response indicates a pole-zero beyond its bandwidth. The high TIA gain is essential for achieving lower input-referred noise current and reduced power consumption, as discussed later.

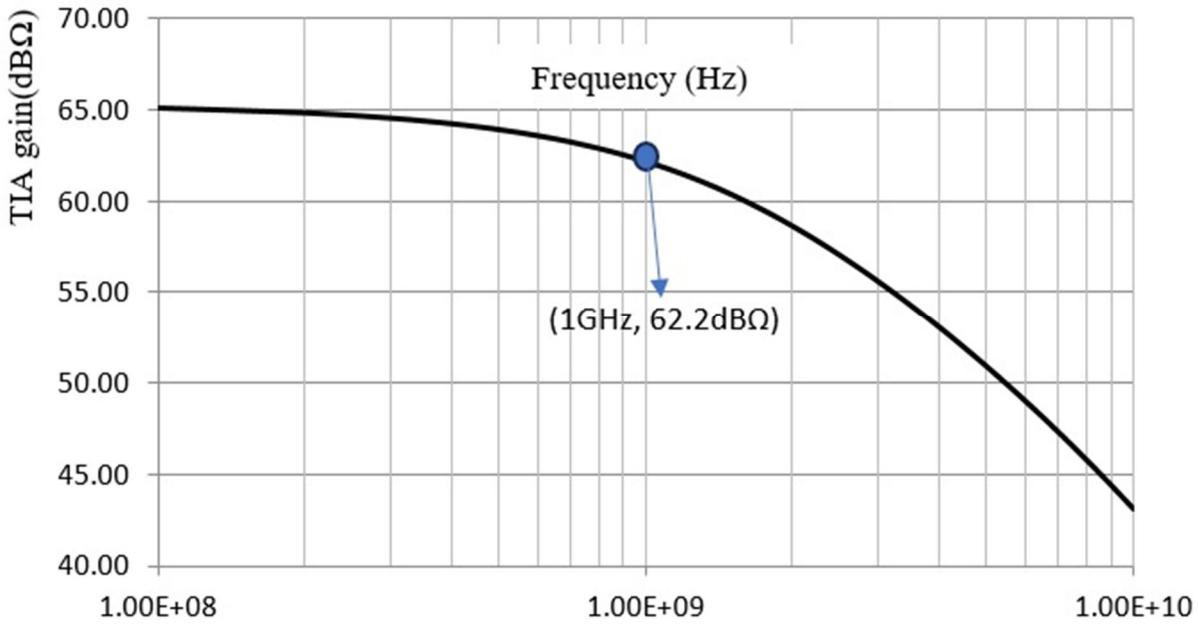

FIG. 5. TIA gain versus signal frequency.

The frequency-dependent input impedance is reported to be 235 Ω at 1 GHz, as shown in Fig. 6. A noticeable peak in the input-impedance nonlinearity occurs at 230 Ω corresponding to a reduced transimpedance amplifier (TIA) gain. It is therefore reasonable to assume that, at midband gain, the input impedance exhibits a near-exponential relationship.

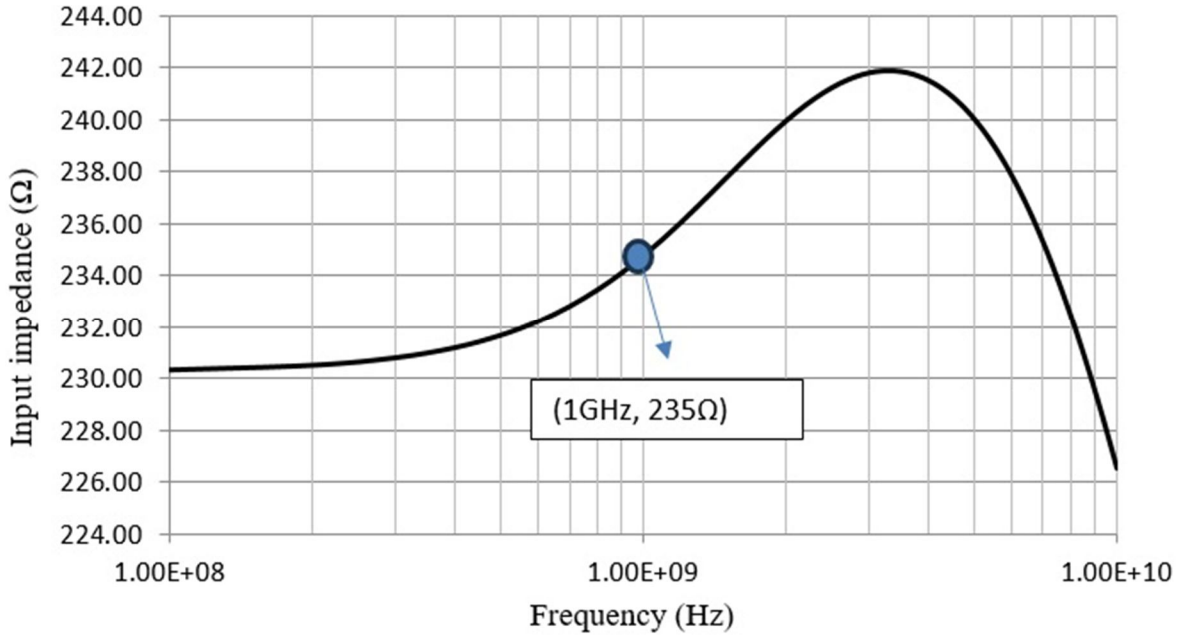

FIG. 6. Input impedance versus signal frequency.

The power consumption of each transistor is given in Fig. 7. The highest power consumption is observed in transistors M_3 and M_{10}, which have connected drains, whereas the lowest power consumption is reported for transistors M_1, M_5, and M_{14}. The average power consumption of the proposed topology is 0.975 mW.

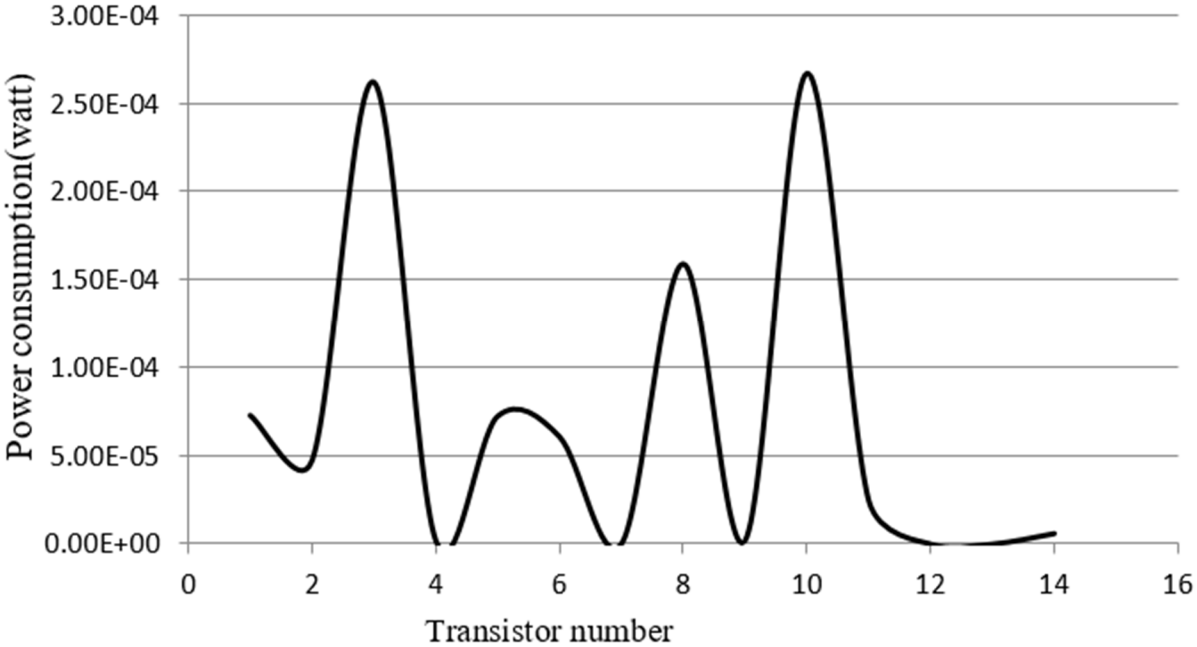

FIG. 7. Power consumption as per each transistor number.

The input-referred noise current spectral density is simulated as in Fig. 8. It can be seen that the input-referred noise decreases as the signal frequency increases. However, this reduction is up to a certain limit after which it starts to rise as the frequency exceeds 10 GHz. The reported input-referred noise current spectral density at the bandwidth point (1 GHz) is around $28\ pA/\sqrt{H_z}$.

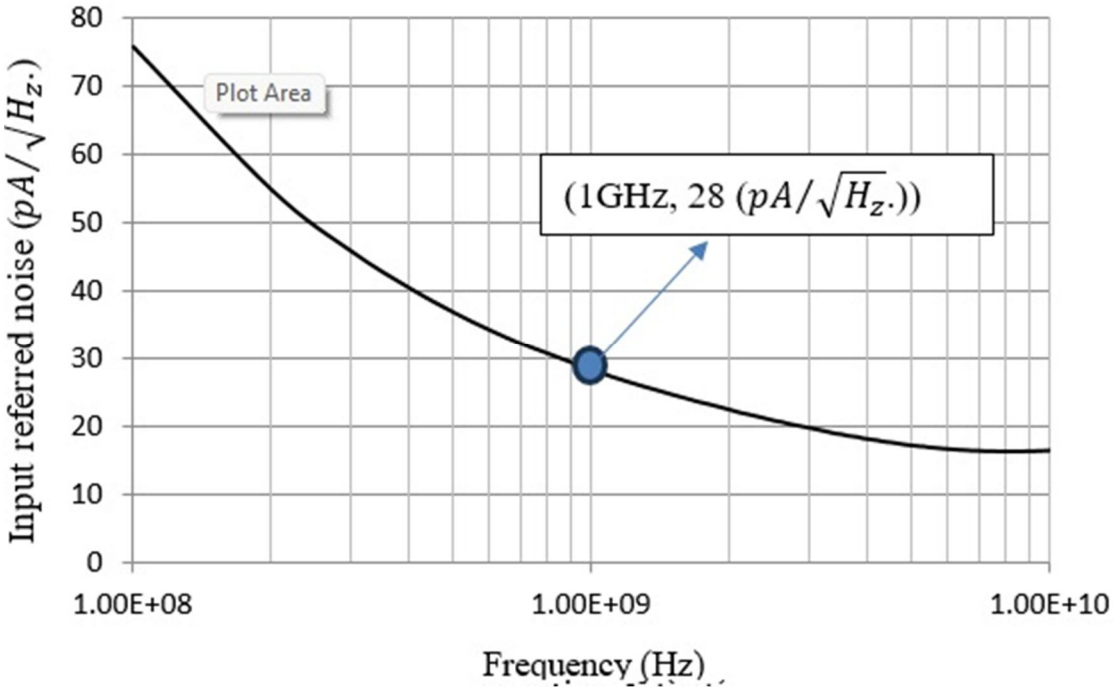

FIG. 8. Input-referred noise current (spectral density) versus signal frequency.

The eye diagram of the proposed 45 nm TIA design is presented in Fig. 9 for a 1 Gbps bit sequence. The trigger clock is initiated at logic level 0 (low), corresponding to 0.34 V, while logic level 1 (high) corresponds to 0.99 V with a rise time of 150 ps.

The slope corresponding to a voltage swing change of 0.91 V over a time interval of 639 ps is sufficiently small, indicating sensitivity to timing errors. The measured jitter is approximately 15 ps and is defined as the variation in the zero-crossing time. Furthermore, the optimum sampling time is approximately 981 ps, corresponding to the decision point at which the eye opening is maximized, thereby providing the best signal-to-noise ratio (SNR). The SNR at the sampling point is approximately 0.32V.

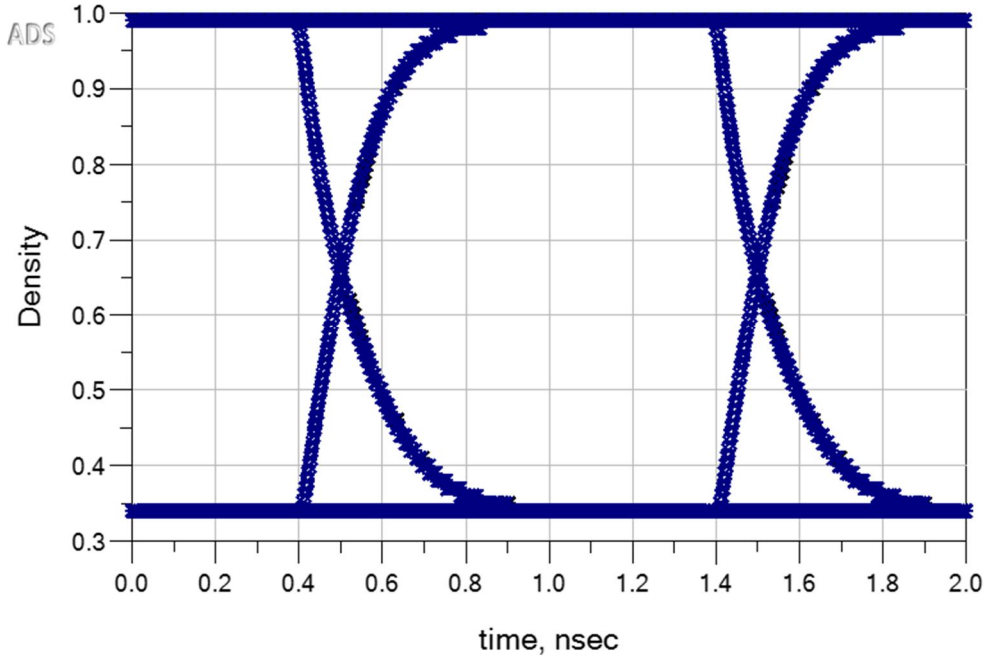

FIG. 9. Eye diagram with bit sequencing at 1 Gb/s.

The reported eye diagram was obtained under the assumption that the signal is stationary, in which its variance and mean value are time-independent. The sampling rate was clearly high

enough to include signal transitions accurately. A 2 ns interval is considered a sufficiently long observation period to have a well-behaved signal. Other assumptions suggest that the measure of jitter and S/N ratio may not necessarily comply accurately with practical measurement. Looking at signal characteristics, there are no apparent signal integrity problems to be considered as a form of limitation. Signal impairments are not masked since eye opening is achieved with remarkable trigger accuracy. The measure of jitter (15 ps) carries no random components; hence, no real constraints are imposed, leading to adjustable jitter. The limitation imposed by Inter Symbol Interference (ISI) that emanates from eye closure does not constitute a significant portion. However, the eye diagram of Fig. 9 does not address signal impairments that are generated due to impedance mismatch between the trigger source and the TIA input impedances. The axis of density represents the frequency of occurrence within the specified voltage levels (already stated in results) at a given time of Fig. 9 per unit interval.

5. Comparative Performance Analysis

Compared to this work, as in Table 1, the TIA gain limitation in terms of trade-offs with other parameters is illustrated with 7.6 dBΩ [18]. Other limitations were manifested by high power consumption of 37 mW [19], while literature reported the bandwidth of 100 MHz [20]. This work shows that although the input-referred noise current spectral density is 28 $pA/\sqrt{H_z}$ which appears to be higher than other literature, however, it is still relatively low compared to application-specific demands and most importantly, with a high TIA gain of 62.2 dB and low power consumption of 0.975 mW. Application-specific demands mainly focus on high impedance sensor interfacing, and to be more specific, applications with high output impedance photodiodes in which the input-referred noise current spectral density becomes a significant contributor to the total output noise. This is due to the fact that the noise current that flows through high source impedance is mainly converted into noise voltage, which contributes to the amplifier's input-referred voltage noise. Therefore, low input-referred noise current is essential in such sensors. Fiber optic communications are major applications that require low input-referred noise in order to detect weak signals ($\sim 100\,\mu A$ utilized in the current study) as this feature is important for long-haul communication where attenuation of signal occurs. High data transmission rates are possible with low noise for which they allow encoding more bits per symbol. Low input-referred noise in such systems enhances the SNR of the signal making it possible to distinguish it from background noise.

The addition of an active inductor feedback impedance illustrates the power consumption performance with clarity, compared to other literature. However, other literature [18-19] with high power consumption is not application-specific. For instance, sub-milliwatt power consumption is hugely important in TIAs employed in short-reach interconnects. Applications such as board-to-board optical links can have very low power consumption requirements. Other applications that involve integrated photonics that can have on-chip electronic and photonic components side by side do achieve reduced parasitic capacitances, leading to lowered on-chip power consumption.

TABLE 1. TIA comparative performance analysis with other literature.

Ref.	[18]	[19]	[20]	This Work
Year	2012	2018	2022	2024
CMOS Technology (nm)	45	45	45	45
TIA Gain (dBΩ)	7.6	74.4	140	62.2
Bandwidth (GHz)	33	23	10 MHz	1
Input-Referred Noise $\left(pA/\sqrt{H_z}\right)$	7.2	1.8μArms	3.38	28
Power Consumption (mW)	9	37	0.01	0.975
DC Supply Voltage (V)	1	1	-	1
No. of Active Inductors	0	0	0	1

6. Discussion

Theoretically, CS configurations represented by transistors M_1 and M_2 (where M_1 simultaneously operates in a CG topology with phase-shifted CS outputs), they draw no current at inputs and therefore have extremely high input impedances and current gains. These high input impedances force the input signal toward the CG input nodes $in1$ with impedances of $1/g_{m1}$ which are extremely low, hence enabling transistors M_1 to conduct with a wide bandwidth. The level of high current gain serves the output of the RGC input stage (being a current gain provider), as well as it serves to stabilize the drain current path when it comes to the CG output nodes for the transistor M_1. The relaxed conduction of M_1 enables $V_{GS2} > V_{TH2}$ for M_2 to conduct in response.

Further to the discussion above regarding the input stage, the PMOS load transistors M_8, M_9, and M_{10} loads exhibit high small-signal resistance. Drain-current paths are established independently of the voltages at the nodes $O1$, X, and Y, respectively. The PMOS loads relax the trade-off between voltage gain and signal headroom, given the fact that, for instance, the voltage gain of the amplifying transistor M_1 is $(-g_{m1}r_{O1})$. The common-source (CS) stage of transistor M_1 as well as in transistor M_2 can have their output resistances r_{O1} and r_{O2} increased without requiring additional power dissipation. The bandwidth of transistors M_1 and M_2 is inherently limited due to high parasitic capacitance resulting from the Miller effect. In essence, the gate-to-drain capacitance is multiplied by a factor of $1 + |A_{v1}|$, thereby increasing the total input capacitance and consequently reducing the bandwidth. For instance, the voltage gain of transistor M_1 in the CS configuration $g_{m1}(r_{O1} \parallel r_{O8})$ is large for large r_{O8}, therefore, a small parasitic capacitance C_{gd1} can have a large impact on the amplifier frequency response and the same applies to transistor M_2. The presence of the common-gate part of transistor M_1 functions as a current follower that has a combined voltage gain effect with a limited input resistance $\approx 1/g_{m1}$. A reduction in r_{O8} effectively decreases the effect of capacitance C_{gd1}. An active inductor exhibits large tunable inductance with high resonance frequency, high quality factor, and a small chip area. This makes the active inductor feedback load is an alternative to spiral inductor load which suffers from voltage transients dependent on di/dt. The negative active inductor feedback process, with an absence of inductive peaking, stabilizes output by reducing voltage fluctuations through modification of input and output impedances. Given that active feedback impedance Z_{f1} as in Eq. (10) is significant at high frequency, its parallel configuration with the input node $in1$ results in a low feedback admittance Y_{f1}, which conducts only a very small fraction of the signal swing back to the input node without considerable fluctuation. This fractional swing is independent of the open-loop voltage gain, which leads to the closed-loop gain being less sensitive to variation in the open-loop gain.

The low input-referred noise current spectral-density contribution is due to the feedback admittance's low magnitude. According to Eq. (15), the value of M is governed by $Y_{f1}r_{ds8} \ll 1$ where higher Z_{O1} leads to minimized mean square channel thermal noise voltage contributed by the drain of the transistor M_1 according to Eq. (25). Additionally, parasitic capacitance C_{gs12} within the active feedback acts as an open circuit at low frequencies causing transistor M_{12} to become diode-connected as the active inductor impedance is approximated as $1/g_{m12}$ following Eq. (10). At high frequencies, the gate of the transistor M_{12} is effectively grounded, whereas the active feedback impedance is near r_{ds13}. This resistance depends on channel length modulation and drain current, and hence current transients do not occur, and therefore preventing unnecessary energy dissipation in transistor M_1. As a result, the total power consumption is reduced to 0.975 mW. In this work, as $r_{ds13} \gg 1/g_{m12}$, tunable active inductor feedback inductance becomes $(r_{ds13}C_{gs12}/g_{m12})$, which contributes to the low power consumption. Tunable inductance also contributes to the alleviation of bandwidth limitations by resonating input parasitic capacitance. It also contributes to an optimum group delay in order to avoid undesirable frequency-response peaking.

The input signal of the subsequent stage at the node A was configured to get into CS mode at the gate of the transistor M_5 which is biased by a transistor M_{14} to increase open-loop gain. The presence of the local active feedback resistor r_{f2} is to control the stage input resistance and

reach its lowest point at which the bandwidth is widest to accommodate the time constant of the input stage output node $O1$. However, a too low r_{f2} value can result in additional induced thermal noise with degraded voltage gain. The common drain transistor M_4 is placed between the stage output and the feedback resistor r_{f2} so that current consumption via this resistor is minimized.

The 0.975 mW low magnitude of power consumption is particularly important at a bandwidth of 1 GHz, TIA gain of 62.2 dBΩ, an input-referred noise current of 28 $pA/\sqrt{H_z}$ at a crucial DC supply voltage of 1V only. Recent RGC-based TIA (90 nm process) literature reported 1 mW of power consumption at 7.3 GHz bandwidth, 50.5 dBΩ of TIA gain, 13.7 $pA/\sqrt{H_z}$ of input-referred noise at 1.2V supply voltage [2]. Recent work on current mirror TIA (90 nm process) suggested 1.08 mW of power consumption at 1 GHz, 66.63 dBΩ of TIA gain, 25.413 $pA/\sqrt{H_z}$ at a 1V DC supply voltage [24, 21]. Other RGC-based TIA (90 nm process) literature [21 22] reported 1.3 mW power consumption at 3.7 GHz of bandwidth, 40.6 dBΩ of TIA gain, 25.3 $pA/\sqrt{H_z}$ of input-referred noise current at a 1.2V supply voltage. Literature that involved current reuse RGC TIA (65 nm process) [22, 23] reported 4.34 mW of power consumption at 10.3 GHz of bandwidth, 65.8 dBΩ of TIA gain with no reported input-referred noise current at a 1.8V supply voltage. In 250 nm process, additional work [23, 24] indicated 831 mW of power consumption at 46.8 GHz of bandwidth, 49.4 dBΩ of TIA gain, with no reported input-referred noise current at a -3.3V supply voltage.

In general, the trade-off between the low bandwidth of 1 GHz and the high TIA gain of 62.2 dBΩ originates from high active inductor impedance following Eq. (10) in conjunction with dominant parallel photodiode capacitance. This configuration enables the creation of a dominant pole with a time constant even at low frequencies. This trade-off is relaxed (alongside low power consumption and input-referred noise) due to minimal phase noise introduced by the input stage current gain amplifier. This means that the input parasitic capacitances played a significant role in suppressing oscillation instability while preventing further bandwidth degradation. The parasitic capacitances associated with the active-inductor feedback provide an inherent frequency-compensation mechanism that sustains the 1 GHz bandwidth value. In contrast, passive feedback capacitors lack this feature due to their unavoidable imposed values.

The active inductor is efficient in terms of a small footprint with tunable inductance compared to an ordinary spiral inductor that occupies a large area on an integrated circuit. This tunability is performed through adjusting bias voltages and currents of PMOS transistors M_{13} and M_{14}. It is therefore possible to improve chip performance through an on-chip adjustment of active inductor feedback (impedance) biasing points. This provides an alternative means of compensating for process variations, such as in the case of passive resistors with low Q-factor, which is normally associated with losses not only by passive resistors but also by passive inductors and their substrates. Device performance is further improved when the PMOS-based active inductors draw less drain current, lowering overall power consumption.

The expected active inductor layout implications in terms of area and process variability can be addressed. The key to establishing an efficient layout is to minimize the length of interconnects with routing that can help minimize parasitic effects associated with gate-source, gate-drain, and drain substrate that can have an impact on the equivalent inductance as well as active inductor frequency response. Chip area in layout work is also affected by specific PMOS transistor sizes in addition to the technology node (e.g., 45 nm). Transistor characteristics can be matched in terms of transconductances g_{m12} and g_{m13}. Normally, active inductor transistors are placed side by side, oriented in a unified direction in order to reduce the effects of process gradients. The width and spacing of metal interconnects affect line resistance and therefore have significant implications for layout-related process variability.

7. Conclusion and Future Work

In conclusion, a relaxed trade-off between low power consumption and high TIA gain was achieved in the simulated proposed design at 45 nm CMOS process technology at a given moderate input-ansistorreferred noise current spectral density with a bandwidth of 1 GHz. The

benefit of the active inductor as local feedback at input stage showed minimal inductive peaking in terms of stabilized TIA gain within its frequency response.

In future work, the photodiode interfacing with TIA input stage can be utilized to improve its response and speed. The photoconductive mode in reverse bias at voltages lower than 1V can be used for faster response time. The parallel configuration between the photodiode and the frequency-dependent input impedance represented by Eq. (11) can be developed even further to enable the input stage current gain to impact the overall TIA gain of Eq. (22). The above-mentioned parallel configuration can have better time constant matching at the photodiode parasitic capacitance/active inductor feedback joint node. One of the key considerations for photodiode interfacing is the reverse bias voltage that suppresses dark current from taking hold, while improving the photoconductive mode. Photodiode junction capacitance can limit its bandwidth. However, more development in trade-off relaxation techniques can further loosen such constraints.

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