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ARTICLE

A Simulated 45 nm MOSFET Channel Process in Transimpedance Amplifier Design for Optoelectronics Applications

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Abstract: A 45-nm metal-oxide-semiconductor field-effect transistor (MOSFET) channel process was simulated in transimpedance amplifier design performance for fiber optics and other major optoelectronics applications. Combined concepts of input stage feedforward followed by a current mirror stage with local active inductor feedback were introduced. The key advantages of this particular design are of great importance, especially in using a PMOS-based local active inductor (feedback formation) instead of a spiral inductor resulting in high transimpedance amplifier (TIA) gain as well as in extremely low power consumption. An overall TIA gain of 68.2 dBΩ was obtained with the f_{-3dB} bandwidth of 2.5 GHz, 0.555 mW of power consumption, and an input-referred noise current spectral density of 31.86 $pA/\sqrt{H_z}$ using a 1V DC budget supply.

Keywords: Transimpdance, Optical preamplifier, Front-end amplifier, Fiber optic TIA.

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1. Introduction

Transistor numbers inside chips have increased over the years because of the shrinking size of MOSFETs. By reducing the source-to-drain spacing, the driving current in the channel increases. In addition, it leads to the short-channel effects (SCEs) [1]. In recent years, there has been a massive increase in demand for low-power and high-performance digital devices. The scaling of CMOS has always beaten predictions and has advanced faster than predicted. The benefits of scaling have been wide-ranging, including decreasing device size, increasing chip and component density, and improving performance and speed [2].

From an optical receivers' point of view, advances within fiber optical networks have witnessed a fast increase in recent years. One methodology used the g_m/I_D approach for the design of regulated cascode (RGC) TIA topology. A framework was introduced that uses lookup tables with this methodology to define the sizing of transistors. This framework sets the limits on the design space and hence provides flexibility to minimize DC power consumption or total input-referred noise. A 130 nm CMOS process was implemented, with 1.5V of supply voltage. A TIA gain of 59.885 dBΩ with a bandwidth of 6.9 GHz, an input-referred noise of 7.925 $pA/\sqrt{H_z}$, and a minimum power of 872.965 μW was obtained under 1.5V supply voltage [3]. An RGC TIA technique involving active inductor peaking, active feedback, and source follower was simulated using a 0.18 μm CMOS process. A TIA gain of 71.51 dBΩ with a bandwidth of 2.2 GHz, an input-referred noise of 8.3 $pA/\sqrt{H_z}$, and a power consumption of 10 mW was achieved under 1.8V supply voltage

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[4]. An RGC TIA input topology with a positive amplifier and an inductor that controls the circuit input impedance and isolates large input parasitic capacitance was introduced. It was implemented using a 1P6M 0.18 µm RF CMOS process. A TIA gain of 58.4 dBΩ with a bandwidth of 4.98 GHz, and a power consumption of 25.24 mW was reported under a 1.8V supply voltage [5]. An inductorless 0.13 µm CMOS TIA was synthesized using an immittance converter that can be configured as either a negative impedance converter to generate an active –C element or a positive impedance converter to generate an active inductance. A TIA gain of 50 dBΩ with a bandwidth of 7 GHz, an input-referred noise of $31pA/\sqrt{H_{z,}}$ and a power consumption of 7 mW was achieved using a 1.5V supply voltage [6]. A regulated common gate TIA based on a third-order elliptic filter approach was introduced. A 0.13 µm CMOS process was implemented. A TIA current gain of 50 dBΩ with a bandwidth of 15 GHz, an input-referred noise of 20 $pA/\sqrt{H_z}$, and a power consumption of 5.34 mW was reported under a 1.2V supply voltage [7]. A common source with active inductor peaking was realized for a 2.5 Gb/s TIA using a 130 nm CMOS process. A TIA gain of 46.16 dBΩ with a bandwidth of 2 GHz, an integrated input-referred noise of 1.062 μA_{rms}, and a power consumption of 5.4 mW was reported under a 1.8V supply voltage [8].

A common source TIA with a shunt feedback resistor and current mirror load was introduced. A TIA gain of 64.5 dBΩ with a bandwidth of 1.05 GHz, an input-referred noise of 16 $pA/\sqrt{H_z}$, and a power consumption of 3.78 mW was reported under a 1.8V supply voltage [9]. A self-cascode TIA structure based on merging transistors (using the same gate biasing) to work as a single transistor was simulated in the TSMC 0.18 µm CMOS process. A TIA gain of 56.8 dBΩ with a bandwidth of 2.7 GHz, an input-referred noise of 11.2 $pA/\sqrt{H_z}$, and a power consumption of 0.42 mW was reported under a 1.8V supply voltage [10].

An inductorless push-pull current mirror TIA followed by a three-stage voltage amplifier and a 50 Ω buffer for 10 Gb/s application implemented in 40 nm CMOS was achieved. A TIA gain of 57.5 dBΩ with a bandwidth of 6.6 GHz, an input-referred noise of 17.5 $pA/\sqrt{H_z}$, and a power consumption of 18.04 mW was reported under a 1.1V supply voltage [11]. Other techniques involved decreasing input resistance due to the use of a diode-connected input stage at the input node, while the output node is enhanced by an active inductive peaking as an output load in order to extend the current-mirror-based TIA bandwidth while keeping the low power consumption performance. A TIA gain of 40.5 dBΩ with a bandwidth of 7 GHz, an input-referred noise of 20.3 $pA/\sqrt{H_z}$, and a power consumption of 1.4 mW was reported under 1V supply voltage [12].

A design methodology to extend bandwidth for RGC TIA with the use of a dual shunt feedback configuration to improve the natural frequency and optimize the damping factor was introduced. The common source auxiliary amplifier is replaced by an inverter amplifier to provide additional gain and reduce equivalent input noise current. A TIA gain of 60.5 dBΩ with a bandwidth of 5.2 GHz, an input-referred noise of 14.99 $pA/\sqrt{H_z}$, and a power consumption of 28.4 mW was reported under a 1.8V supply voltage [13]. A 30 Gb/s 0.18 µm CMOS TIA which incorporates three-stage differential amplifiers with active negative feedback was introduced. A TIA gain of 45 dBΩ with a bandwidth of 21.23 GHz, an input-referred noise of 63.1 $pA/\sqrt{H_z}$, and a power consumption of 10.296 mW was reported under a 1.8V supply voltage [14].

The purpose of this work is to combine the above concepts in a front-end topology in which a modified RGC (feedforward input stage) followed by a current mirror stage with local active inductor feedback is introduced, in order to reduce power consumption while maintaining high TIA gain.

1.1 Feedforward Transimpedance

In Fig. 1(a), transistor M_2 operates as a common gate stage and, also being in a feedback loop, it works as a source follower. Resistor R_2 is equivalent to the overall transimpedance amplifier (TIA) gain at low frequencies. If the loop at the M_2 gate is broken, provided that body effect and channel length modulation are neglected, the input resistance is represented by [15]:

$$R_{in} = \frac{1}{g_{m2}}\left(\frac{1}{1+g_{m1}R_1}\right) \quad (1)$$

where g_{m1} and g_{m2} are the transconductance parameters for transistors M_1 and M_2,

respectively. Due to the feedback loop, the input resistance is lowered; hence, the bandwidth is extended. The circuit in Fig. 1(a) can be redrawn as in Fig. 1(b) which is basically a feedforward amplifier that drives the gate of transistor M_2, which is in a common source formation.

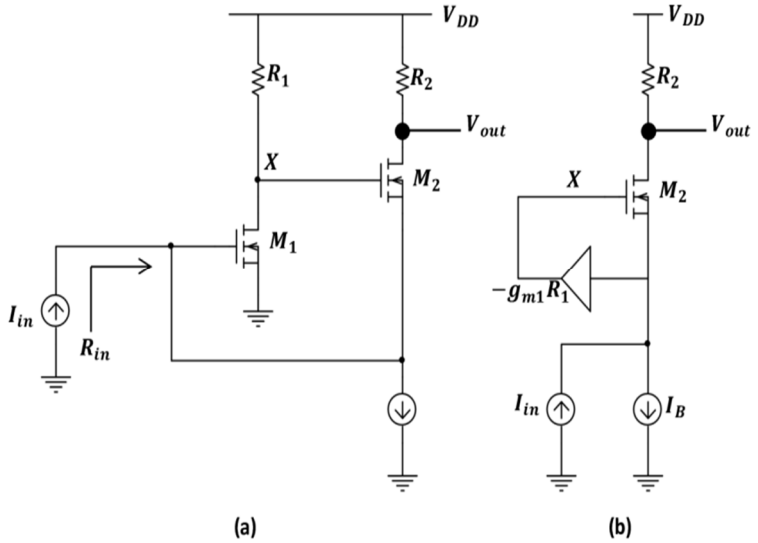

FIG. 1. (a) TIA in feedback form, (b) Amplifier inserted in feedforward path [15].

1.2 Current Mirror Topology

The fundamental current mirror topology consists of two MOSFET transistors, M_1 and M_2, as shown in Fig. 2. Both transistors operate in saturation mode in which the output current I_{OUT} has a direct relationship with I_{REF}. The drain current I_{D1} is a function of V_{GS1} and V_{DG1} based on the MOSFET functionality. The known current I_{REF} is the drain current of transistor M_1. It can be supplied by a resistor or by a threshold-referenced current source to make sure that it is constant regardless of variations in supply voltage [16].

Transistor M_1's drain current is $I_{D1} = f(V_{GS1}, V_{DG1} = 0)$, in which $f(V_{GS1}, 0) = I_{REF}$, thus determining the V_{GS1} value (i.e., I_{REF} determines the V_{GS1} value). The same value of V_{GS1} is forced upon transistor M_2.

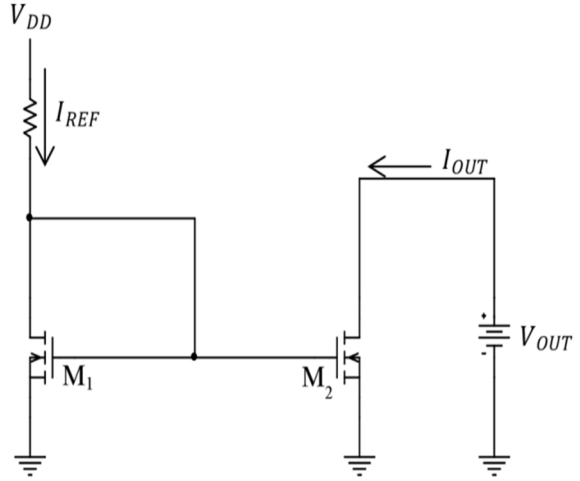

FIG. 2. An n-channel MOSFET current mirror topology [16].

2. Proposed TIA Topology

In Fig. 3, the planned TIA design is simulated using LTspice XVII with a 45 nm Predictive Technology Model (PTM). The feedforward input stage consists of NMOS amplifying transistor M_1 with an M_2 transistor that provides DC voltage level shifting for NMOS transistor M_3. This level shifting facilitates V_{gs3} accommodation, allowing greater voltage headroom to hasten the M_3 drain sinking current.

In a local feedback form, the M_1 NMOS transistor displays limited voltage amplification from node *N* to node O_1. For this particular input stage, a better transconductance can be achieved for transistors M_1 and M_3 since their gate-to-source voltages are given enough headroom to operate. PMOS current sources (transistors M_5, M_6, and M_7) provide stable drain current paths as the feedforward input stage is a development of earlier literature [17].

Identical device dimensions in transistors M_8 and M_9 enable drain current mirroring to the output node O_2. In the current mirror stage, channel length modulation determines the operation of transistor M_7 (current source). Consequently, drain current I_{O2} equals the drain current of transistor M_7 at the value of V_{O2} which causes transistors M_8 and M_9 to have $V_{DS8} = V_{DS9}$. The presence of the PMOS-based local active inductor (as with transistors M_{11} and M_{12} configuration) minimal impacts current mirror operation having minimal voltage feedback to the gates of transistors M_8 and M_9.

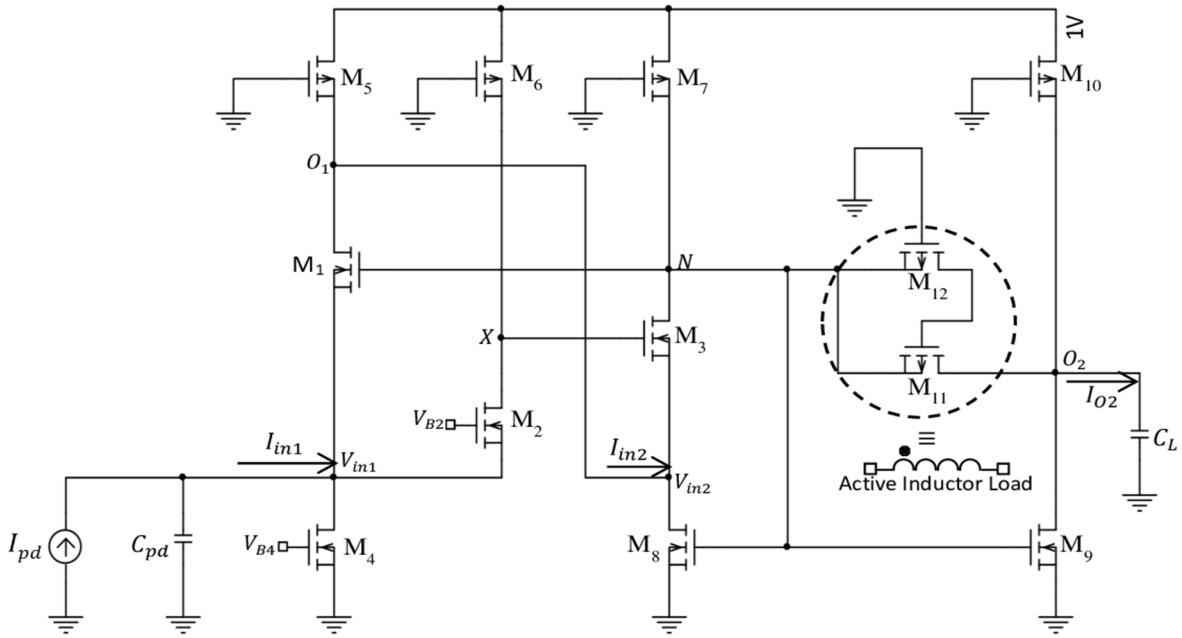

FIG. 3. Proposed TIA topology.

A portion of the feedback signal voltage swing is effectively dropped on node *N* which not only determines the gate voltages for transistors M_8 and M_9 but also controls the gate voltage of transistor M_1. In practice, $V_{O2} \approx V_{gs8} = V_{gs9}$ and as V_{O2} increases, I_{O2} also increases based on the incremental output resistance r_{o9} of transistor M_9, represented as $R_{O2} = \Delta V_{O2}/\Delta I_{O2} = r_{o9} = V_{A9} / I_{O2}$. The early voltage V_{A9} of transistor M_9 is proportional to the transistor channel length (65 nm) which has a finite nature.

Further circuit design analysis in Fig. 3 shows that transistor M_3 serves multiple roles. Firstly, in the input stage, it is configured in the common source (CS) topology which has a gate-to-source voltage to be overcome easily due to the DC voltage level rising at node *X* provided by the pass transistor M_2. Secondly, transistor M_3 has a mutual interface between the input stage and the current mirror stage in the form of a common gate (CG) topology with input current I_{in2} supplied by node O_1. Finally, the drain of transistor M_3 at node *N* is a common node that receives amplified signals from the CS and CG topologies mentioned earlier.

2.1 A 45 nm MOSFET Process Design

Continual gate oxide scaling requires high-κ gate dielectric (κ being the dielectric constant) since the gate oxide leakage in SiO_2 increases with reduced physical thickness and SiO_2 runs out of atoms for further scaling. The use of high-κ serves the dual purpose of scaling the device as well as reducing gate leakage. Hence, high-κ gate transistors serve as a good alternative to classical CMOS transistors in nanoscale technologies [2]. In this work, a gate length of 45 nm is utilized with a custom PTM (.model level = 54) based on the Arizona State University model as presented in Table 1.

TABLE 1. MOSEFT process-related parameter values.

Parameter	Description Process-related Parameters	(NMOS) Value	(PMOS) Value	Unit
TNOM	Temperature	27	27	C°
EPSROX	Relative gate dielectric constant	3.9 (SiO2)	3.9 (SiO2)	-
TOXE	Electrical gate equivalent oxide thickness	1.75e-09	1.85e-09	m
TOXP	Physical gate equivalent oxide thickness	1.1e-09	1.1e-09	m
VSAT	Saturation velocity	147390	70000	m/s
XJ	Source / Drain junction depth	2e-08	1.4e-08	m

2.2 Input Stage Transimpedance

A small signal model is envisaged for the feedforward TIA input stage in the proposed TIA design, illustrated in Fig. 4. Some important values such as r_{dsx}, C_{dx} and C_{gx} were not possible to neglect. Table 2 provides transconductance parameters for each transistor, while Table 3 presents the aspect ratio (W/L) corresponding to each transistor.

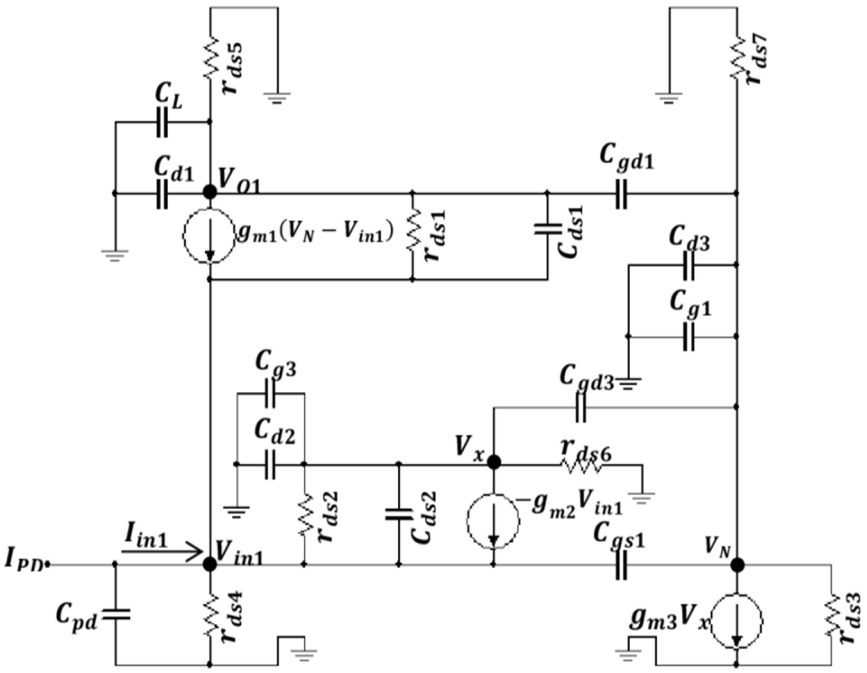

FIG. 4. Small signal model for the feedforward input stage.

TABLE 2. Transconductance parameters for the input stage transistors.

Transistor No.	M_1	M_2	M_3	M_4	M_5	M_6	M_7
g_m/mS	0.40	1.93	1.54	0.158	0.168	0.276	0.169

TABLE 3. Aspect ratio (W/L) for each transistor.

Transistor No.	M_1	M_2	M_3	M_4	M_5	M_6	M_7
W/L	40	43.3	40	28.8	5	10	10

To analyze a systematic voltage gain of this stage, the voltage gain of transistor M_1 is:

$$A_{M_1} = \frac{g_{m1}}{g_{ds5}+g_{ds1}+s(C_{d1}+C_{L1})} \quad (2)$$

Drain-to-source conductances g_{ds5} and g_{ds1} are of transistors M_5 and M_1, respectively, $C_{d1}$is the drain-to-bulk capacitance for transistor M_1, and C_{L1} is the load capacitance at the feedforward stage output. The voltage gain of transistor M_2 is expressed as:

$$A_{M_2} \approx \frac{g_{m2}+g_{mb2}+g_{ds2}}{g_{ds6}+g_{ds2}+s(C_{d2}+C_{g3})} \quad (3)$$

The bulk transconductance parameter g_{mb2} is for transistor M_2, while C_{g3} is the gate to the bulk capacitance of transistor M_3.

Whereas the voltage gain of transistor M_3 is given as:

$$A_{M_3} \approx \frac{g_{m3}}{g_{ds7}+g_{ds3}+s(C_{d3}+C_{g1})} \quad (4)$$

The overall voltage gain of the input feedforward stage (first stage) is represented by:

$$A_{v1} = \frac{V_{O1}}{V_{in1}} \approx A_{M_1}\left[1 + \left|A_{M_2}A_{M_3}\right| + \frac{1}{g_{m1}}(g_{mb1} + g_{ds1})\right] \quad (5)$$

In Eq. (5), the voltage gain is increased by a factor of $\left(1 + \left|A_{M_2}A_{M_3}\right| + \frac{1}{g_{m1}}(g_{mb1} + g_{ds1})\right)$. The input impedance of this stage is expressed as:

$$Z_{in1} = \frac{1}{\beta+sC_{EQ}} \quad (6)$$

For which,

$$\beta = g_{m1}\left(1 + \left|A_{M_2}A_{M_3}\right|\right) + g_{ds2}(1 - A_{M_2}) + g_{ds1}(1 - A_{v1}) + g_{mb1} + g_{m2} + g_{mb2} + g_{ds4} \quad (7)$$

The equivalent input stage capacitance is

$$C_{EQ} = \left[C_{i,tot} + \left|A_{M_2}A_{M_3}\right|C_{gs1}\right] \quad (8)$$

where $C_{i,tot}$ is the total input capacitance dominated by the photodiode input capacitance C_{pd}, whereas the input resistance in terms of DC level is $R_{in1} = 1/\beta$ as the bandwidth is expressed as:

$$f_{-3dB} = \frac{\beta}{2\pi C_{EQ}} \quad (9)$$

The TIA gain of the input stage is:

$$Z_{TIA1} = \frac{A_{v1}}{\beta+sC_{EQ}} \quad (10)$$

The reduced input impedance in combination with high voltage gain leads to the enhancement of the TIA gain of this particular stage. The output impedance of this stage is:

$$Z_{O1} = \frac{1}{(g_{ds2}+g_{ds6})+s(C_{d2}+C_{g3}+C_{ds2}+C_{gd3})} \quad (11)$$

where C_{ds2} is the drain-to-source capacitance of transistor M_2, while C_{gd3} is the gate-to-drain capacitance of transistor M_3.

The output/input currents (I_{O1}/I_{in1}) can be expressed as:

$$\frac{I_{O1}}{I_{in1}} = \frac{Z_{TIA1}}{Z_{O1}} \quad (12)$$

2.3 Current Mirror Transimpedance

The small signal equivalent circuit of the current mirror stage with local active inductor feedback is illustrated in Fig. 5.

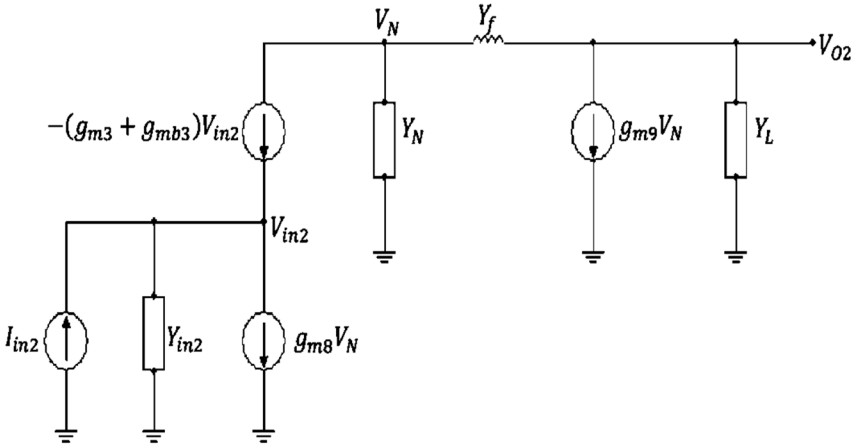

FIG. 5. Small signal model of the current mirror stage.

Following the KCL nodal analysis of Fig. 5, the following equations are obtained:

$$V_{O2}Y_L + g_{m9}V_N = (V_{O2} - V_N)Y_f \quad (13)$$

$$V_N Y_N - (g_{m3} + g_{mb3})V_{in2} = (V_{O2} - V_N)Y_f \quad (14)$$

$$I_{in2} - V_{in2}Y_{in2} - (g_{m3} + g_{mb3})V_{in2} = g_{m8}V_N \quad (15)$$

With regard to the current mirror stage, V_{O2} is the output voltage of the TIA circuit, Y_L is the load admittance, V_N is the node N voltage, Y_f is the local feedback admittance, I_{in2} and V_{in2} are the input current and voltage, respectively, and Y_{in2} is the input admittance of this stage.

The voltage gain of the current mirror stage (second stage) is:

$$A_{v2} = \frac{V_{O2}}{V_{in2}} = \frac{(g_{m3}+g_{mb3})(Y_f+g_{m9})}{[(Y_f+Y_L)(Y_f-Y_N)-Y_N(Y_f+g_{m9})]} \quad (16)$$

The TIA gain of the current mirror stage with local active inductor feedback is represented as:

$$Z_{TIA2} = \frac{V_{O2}}{I_{in2}} = \frac{(g_{m3}+g_{mb3})(Y_f-g_{m9})}{P+Q} \quad (17)$$

where,

$$P = g_{m8}(g_{m3}+g_{mb3})(Y_L+Y_f)(Y_f-g_{m9})$$

$$Q = [(Y_L+Y_f)(Y_f-Y_N)-Y_f(Y_f-g_{m9})](Y_{in2}-g_{m3}-g_{mb3})(Y_f+g_{m9})$$

The active inductor feedback admittance Y_f is defined through the inversion of the feedback impedance within the current mirror stage [15]:

$$Z_f(s) = \frac{r_{o12}C_{gs11}s+1}{g_{m11}+C_{gs11}s} \quad (18)$$

The load admittance Y_L at node O_2 is represented as $Y_L = s(C_L + C_{d9} + C_{sbp10})$. At node N, the admittance Y_N is defined through the representation: $Y_N = s(C_{g1} + C_{g8} + C_{g9} + C_{d3})$, whereas Y_{in2} which is the current mirror stage input admittance is expressed as

$$Y_{in2} = s(C_{d1} + C_{sbp5} + C_{s3} + C_{d8}).$$

2.4 Overall TIA Gain Formula

The overall TIA gain formula for the proposed topology is given as:

$$Z_{TIA} = \frac{V_{O2}}{I_{in1}} = \frac{I_{O1}}{I_{in1}} \times \frac{V_{O2}}{I_{in2}} \quad (19)$$

The above formula is based on the fact that $I_{O1} = I_{IN2}$ when multiplying Eq. (12) by Eq. (17).

2.5 Noise Analysis

The drain and gate noise currents are modeled according to the following expressions [17]:

$$\overline{I_d^2} = \widehat{I_d}^2 = 4kT\alpha g_m \quad (20)$$

$$\overline{I_g^2} = \widehat{I_g}^2 = 4kT\delta g_g \quad (21)$$

where α is expressed as $\gamma\, g_{d0}/g_m$, γ is the channel thermal noise coefficient, δ is the gate noise coefficient, $\overline{I_d^2}$ is the mean square channel noise current, $\overline{I_g^2}$ is the gate noise (induced) current. The rms channel and induced current noise densities are $\widehat{I_d}$, $\widehat{I_g}$, respectively. Transistors M_1, M_2, and M_3 produce a mean-square thermal noise (spectral density) voltage as follows:

$$\overline{V_{n,d1}^2} = \left(\widehat{I_{d1}}(Z_{in1}A_{v1} - Z_{O1})\right)^2 = 4kT\alpha g_{m1}(Z_{TIA1} - Z_{O1})^2 \quad (22)$$

$$\overline{V_{n,d2}^2} = \left(\widehat{I_{d2}}(Z_{in1}A_{v1} - Z_xA_{xO1})\right)^2 = 4kT\alpha g_{m2}(Z_{TIA1} - Z_xA_{xO1})^2 \quad (23)$$

$$\overline{V_{n,d3}^2} = \left(\widehat{I_{d3}}Z_NA_{NO1}\right)^2 = 4kT\alpha g_{m3}(Z_NA_{NO1})^2 \quad (24)$$

Voltage gain A_{xO1} is from node X to node O_1, while gain A_{NO1} is from node N to node O_1. Equation (24) represents a significant leap compared to previous literature [17]. The parallel configuration around node N significantly determines the drain noise voltage of transistor M_3 and impacts power consumption, as discussed in Section 4. The output impedance Z_N at node N is an inversion of the admittance $Y_N = s(C_{g1} + C_{g8} + C_{g9} + C_{d3})$. Transistors M_1, M_2, and M_3 also generate an induced gate noise voltage (spectral density) in a mean square form as:

$$\overline{V_{n,g1}^2} = \left(\widehat{I_{d1}}(Z_{in1}A_{v1} + Z_NA_{NO1})\right)^2 = 4kT\alpha g_{m1}(Z_{TIA1} - Z_{O1})^2 = 4kT\delta\frac{\omega^2C_{01}^2}{g_{d01}}(Z_{TIA1} - Z_NA_{NO1}) \quad (25)$$

Given that the shunt conductance for transistor M_1 is $g_{g1} = \omega^2C_{01}^2/g_{d01}$, the induced gate noise current spectral density in Eq. (25) is reformed with regard to the gates of transistors M_2 and M_3 as follows:

$$\overline{V_{n,g2}^2} = \left(\widehat{I_{g2}}Z_{in1}A_{v1}\right)^2 = 4kT\delta\frac{\omega^2C_{02}^2}{g_{d02}}(Z_{TIA1})^2 \quad (26)$$

$$\overline{V_{n,g3}^2} = \left(\widehat{I_{g3}}Z_xA_{xO1}\right)^2 = 4kT\delta\frac{\omega^2C_{03}^2}{g_{d03}}(Z_xA_{xO1})^2 \quad (27)$$

The gate-oxide capacitance is expressed as C_{0x}, while g_{d0x} is the zero-bias drain conductance of transistor M_x. Hence, the mean square drain and gate-induced noise voltages are:

$$\overline{V_{n,Mx}^2} = \overline{V_{n,dx}^2} + \overline{V_{n,gx}^2} + +2|c|\sqrt{\overline{V_{n,dx}^2}.\overline{V_{n,gx}^2}} \quad (28)$$

where c is the cross-correlation coefficient between the drain and the gate noise, $\overline{V_{n,dx}^2}$ is the drain mean-square thermal noise (spectral density) voltage, and $\overline{V_{n,gx}^2}$ is the mean square induced gate noise voltage (spectral density) for

a particular transistor. The noise fraction of transistor M_4 as a current source is:

$$\overline{V_{n,M4}^2} = 4kT\frac{Z_{in1}^2 A_{O1}^2}{r_{ds4}} = \frac{Z_{TIA1}^2}{r_{ds4}} \quad (29)$$

The load resistors' noise fraction is expressed as follows:

$$\overline{V_{n,r}^2} = 4kT\left(\frac{Z_{O1}^2}{r_{ds5}} + \frac{Z_X^2 A_{XO1}^2}{r_{ds6}} + \frac{Z_N^2 A_{NO1}^2}{r_{ds7}}\right) \quad (30)$$

The total TIA output noise voltage is:

$$\overline{V_{n,out}^2} = \overline{V_{n,M1}^2} + \overline{V_{n,M2}^2} + \overline{V_{n,M3}^2} + \overline{V_{n,r}^2} \quad (31)$$

The input-referred noise as spectral density current is:

$$\overline{I_{n,in1}^2} = \frac{\overline{V_{n,out}^2}}{Z_{TIA1}^2} \quad (32)$$

Minimizing the input-referred noise relies on lowering transconductances and output impedances and raising voltage gains A_{v1}, A_{xO1}, and A_{NO1}.

3. Results

The simulated overall TIA gain, transient analysis, and noise performance were obtained using LTspice XVII software. Customized predictive technology models for NMOS and PMOS transistors were utilized, including parameters related to the technology node.

3.1 Overall TIA Gain

The proposed topology achieves an overall TIA gain of 68.2 dBΩ with a f_{-3dB} bandwidth of 2.5 GHz, as shown in Fig. 6.

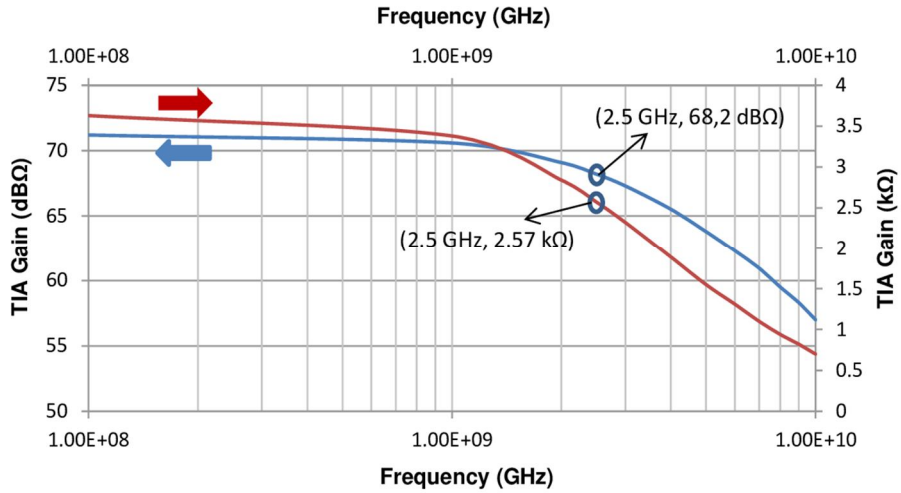

FIG. 6. The overall TIA gain in dBΩ and kΩ.

The f_{3dB} bandwidth (2.5 GHz) complies to a great extent with Eq. (9). A 2.57 kΩ of TIA gain that corresponds to the 68.2 dBΩ is shown in Fig. 6. An input impedance of 174.6 Ω at the f_{3dB} bandwidth is depicted in Fig. 7. The simulated DC transfer function data is given in Table 4, while Table 5 illustrates power consumption as per each transistor with a total of 0.555 mW.

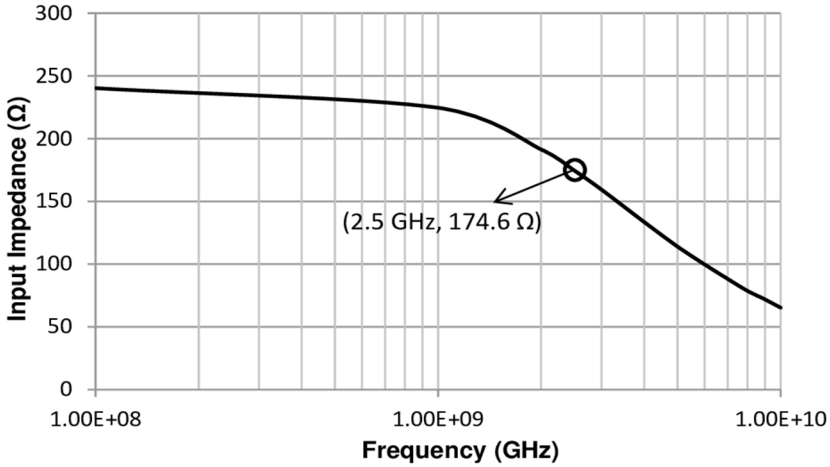

FIG. 7. Input impedance for the proposed circuit.

TABLE 4. DC Transfer Function of the proposed TIA.

Transfer Function	-3638.51
I_{pd} Source Input Impedance	240.422 Ω
Output Impedance at O_2 Node	3286.67 Ω

TABLE 5. Power consumption as per each transistor with a total of 0.555 mW.

M_1	M_2	M_3	M_4	M_5	M_6
3.19 µW	66.34 µW	69.98 µW	15 µW	93.56 µW	83.4 µW
M_7	M_8	M_9	M_{10}	M_{11}	M_{12}
35 µW	73.4 µW	54.82 µW	125.92 µW	3.5 nW	3.5 nW

The key factors influencing the overall TIA gain are the TIA gain of both input and current mirror stages with the output impedance of the input stage according to Eqs. (11), (12), and (17). Figure 8 shows the frequency response of the TIA gain of both feedforward input (TIA1) and current mirror (TIA2) stages, while Fig. 9 illustrates the output impedance of the feedforward stage as a function of input signal frequency. A 1.375 kΩ of output impedance was obtained at the f_{-3dB} bandwidth.

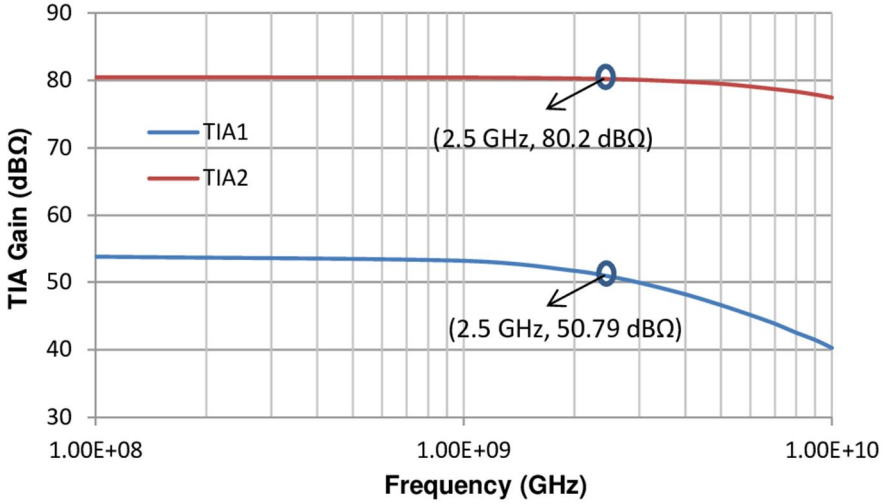

FIG. 8. TIA gain of input and current mirror stages.

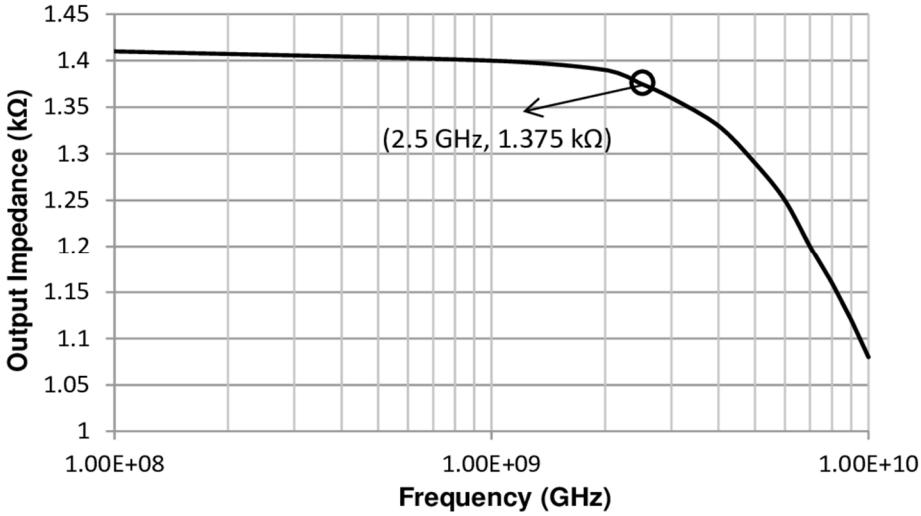

FIG. 9. Output impedance of the feedforward input stage dependence on signal frequency.

According to Eq. (18), the local active inductor feedback impedance mentioned earlier (PMOS-based by transistors M_{11} and M_{12}) is numerically calculated as a function of input signal frequency and is displayed in Fig. 10. A huge magnitude of resistance is reported at the f_{-3dB} bandwidth of 2.5 GHz which will be discussed in Section 4.

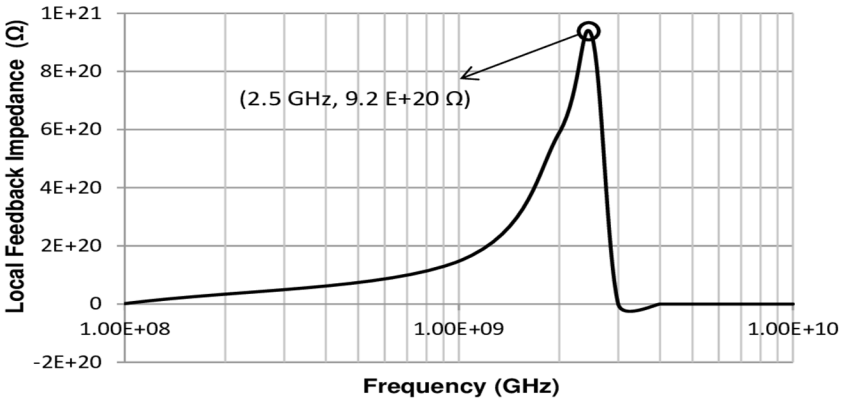

FIG. 10. Numerical calculation of the local active inductor feedback impedance versus signal frequency.

3.2 Transient Analysis

In Fig. 11, a 2.5 Gb/s eye diagram for the proposed TIA is simulated. An input current signal of 100 µA with a nonlinear simulation of 10 µs (stop time) and a maximum timestep of 150 ps is applied. The distortion amount (set by the signal-to-noise ratio) was about 3 mV. At the sampling point, the signal-to-noise ratio was 108 mV. At the decision point which is the optimal time to sample, the signal-to-noise ratio was about 29.51 ps (best signal-to-noise ratio), representing the most open part of the eye diagram. The magnitude of the jitter was about 29 ps. This is suitable for $2^{15} - 1$ NRZ PRBS application.

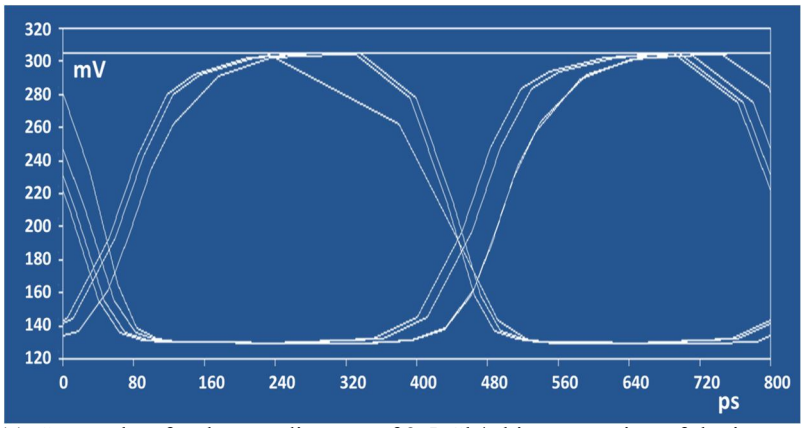

FIG. 11. Screenshot for the eye diagram of 2.5 Gb/s bit sequencing of the input signal.

3.3 Noise Performance

In Fig. 12, the input-referred noise current spectral density is simulated as a function of input signal frequency. A 31.86 $pA/\sqrt{Hz}$ is reported at the f_{-3dB} bandwidth. The lowest levels of input-referred noise are within the range from 1GHz – 2.5GHz.

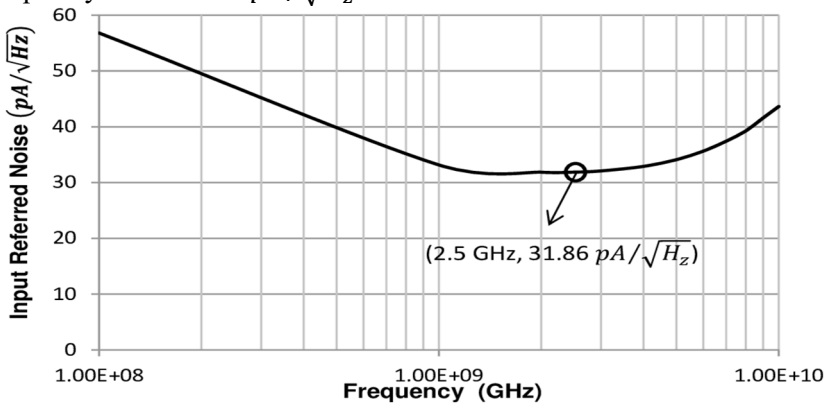

FIG. 12. Simulated input-referred noise current spectral density versus signal frequency.

3.4 Comparative Performance Analysis

The importance of this work becomes apparent when a comparative performance analysis with other research works is presented in Table 6. It is obvious that a key factor difference is the power consumption while maintaining a competitively high TIA gain at a 1V DC supply budget as far as this work is concerned. That would be advantageous for 2.5 Gbps applications with other parameters that proved reasonable such as input-referred noise current spectral density. It is noticed from the performance of other works that high TIA gain often requires high power consumption. This concept can be a significant drawback despite wider bandwidths. Table 7 provides a comparison in terms of complexity versus power consumption between the proposed TIA topology and other research works, as discussed in Section 4.

TABLE 6. Comparative performance analysis with other research works.

Ref.	[18]	[19]	[20]	[21]	[22]	This Work
Year	2016	2017	2017	2020	2020	2022
Technology (CMOS)	0.18 µm	0.18 µm	90 nm	65 nm	55 nm	45 nm
TIA Gain (dBΩ)	55-69	59	41	73.1	69	68.2
Bandwidth (GHz)	1	7.9	3.4	10.2	10.7	2.5
Input-Referred Noise $pA/\sqrt{H_z}$	9.33	23	13.1	30.5	15	31.86
Power Consumption (mW)	6	18	1.4	9.6	15.7	0.555
No. of Passive Inductors	0	2	0	0	0	0
Supply Voltage (V)	1.8	1.8	1	1.2	2.5	1

TABLE 7. Comparative performance analysis of the proposed TIA circuit complexity versus power consumption with other research work.

Ref.	[18]	[19]	[20]	[21]	[22]	This Work
Year	2016	2017	2017	2020	2020	2022
Technology (CMOS)	0.18 µm	0.18 µm	90 nm	65 nm	55 nm	45 nm
Power Consumption (mW)	6	18	1.4	9.6	15.7	0.555
No. of Passive Inductors	0	2	0	0	0	0
No. of Active Inductor Feedback Loops	0	0	0	0	0	1
No. of Passive Resistors	3	0	1	4	2	0
No. of Amplifier Stages	2	2	2	2	2	2
No. of Transistors	10	6	10	10	8	12

4. Discussion

The proposed TIA system performance was envisaged based on significant power consumption reduction. Having Eq.(19), the overall TIA gain is influenced by a current gain provider (feedforward input stage) in the form of I_{O1}/I_{n1} multiplied by a transimpedance gain provider (current mirror stage) in the form of V_{O2}/I_{in2} leading to power consumption reduction which provides the basis for a general inductorless system design that contains a current gain followed by transimpedance gain topologies. Due to the presence of PMOS current sources, M_5, M_6, and M_7, a relaxed trade-off occurs between signal headroom and voltage gain hence enabling fast sinking of drain current for M_1, M_2, and M_3 (less energy storage). There is no effective transient voltage dependence on (di/dt) with regard to the drain current of current sources M_5, M_6, and M_7, hence, these current sources are not considered to be storage elements that consume more power and have longer time laps to discharge. Moderate values of aspect ratios (W/L) and hence transconductances parameters (g_m) for NMOS transistors M_1, M_2, and M_3 enable moderate drain currents which are relatively low and hence lower power consumption compared to data established in comparative results as in Table 6 given that in this work, the DC budget supply is 1V. Another crucial factor in power consumption reduction is the parallel configuration of very high impedances (gate impedance of NMOS transistor M_1 and active inductor impedance by PMOS transistors M_{11} and M_{12}) with the output resistance r_{o3} and r_{o7} given additional parallel gate impedances of M_8 and M_9 (very high) having node N to be the joint node of all mentioned impedances. Only finite (although high enough) resistances (r_{o3} and r_{o7}) will come

into operation (less power-consuming) since the lower drain current of transistor M_3 (from a small signal point of view) is utilized.

Further analysis of the overall TIA gain [Eq. (19)] shows that the current gain of the input stage as described in Eq. (12), partly depends on an inverse relation with the output impedance Z_{O1} of this stage, given in Eq. (11). In this equation, parasitic capacitances admittance term $s(C_{d2} + C_{g3} + C_{ds2} + C_{gd3})$ is significantly smaller than $(g_{ds2} + g_{ds6})$. However, conductances g_{ds2} and g_{ds6} are directly proportional to the current gain (I_{O1}/I_{in1}) as parasitic capacitance constraints still play a role, as depicted in Fig. 9, and cannot be neglected.

At low frequencies, the dominance of conductances g_{ds2} and g_{ds6} becomes apparent as the role of parasitic capacitance admittance $s(C_{d2} + C_{g3} + C_{ds2} + C_{gd3})$ fades away. In addition, Eq. (12) indicates that the current gain of the input stage is directly proportional to its transimpedance gain TIA1 defined in Eq.(11). The TIA2 gain of the current mirror stage is enhanced by g_{m3} and g_{m9} in such a way that $(-g_{m3}r_{o3})$ and $(-g_{m9}r_{o9})$, which are the intrinsic gain of transistors M_3 and M_9, respectively, implicitly control the current mirror voltage gain and subsequently TIA2, as described in Eqs. (16) and (17).

Numerical calculations of the local active inductor feedback impedance of Fig. 10 confirm the f_{-3dB} bandwidth of 2.5 GHz, corresponding to the 68.2 dBΩ of the overall TIA gain. The behavior of the active inductor feedback impedance conforms to that of an ordinary spiral inductor up to 2.5 GHz but deviates beyond the f_{-3dB} bandwidth. This explains the rapid decline of the overall TIA gain beyond the bandwidth point, as shown in Fig. 6. The poles' time constants at nodes N and O_2 govern the frequency response of the active inductor impedance in Fig. 10. However, the rapid decline in impedance and subsequently in TIA gain indicates the presence of a pole *zero* that cancels the dominant pole effect beyond 2.5 GHz. However, there was no obvious inductive peaking in the transimpedance of Fig. 6, indicating that the poles' time constants at nodes N and O_2 are important for an active inductor. Interestingly, the input impedance of Fig. 7 does not exhibit capacitive peaking because the dominant pole frequency of $|A_{M2}A_{M3}|$ is higher than that of the input impedance pole $(g_{m1} + g_{m2})/C_{i,tot}$.

The input-referred noise current spectral density of Fig. 12 could not have been traded off for higher TIA gain and lower power consumption as the magnitude of 31.86 $pA/\sqrt{H_z}$ does not constitute an abnormal value and falls within accepted levels (see Table 6), given the DC supply voltage of 1V. This low supply voltage presents a technical challenge for providing enough voltage signal headroom for the amplifying transistors.

When comparing circuit models in Table 6 in terms of TIA gain, f_{-3dB} bandwidth, and input-referred noise current, it is noticed that short-channel device topologies (65, 55, and 45 nm as in this work) exhibit a rise in TIA gain, f_{-3dB} bandwidth, and input-referred noise compared to the 0.18 µm scale topology given in the literature [18]. However, the 90 nm scale topology shows a decrease only in TIA gain, but an increase in f_{-3dB} bandwidth and input-referred noise compared to the 0.18 µm scale topology given in Ref. [18]. The other 0.18 µm scale topology detailed in Ref. [19] behaves similarly to the 90 nm scale topology when both compared to the 0.18 µm scale topology given in Ref. [18]. The discrepancies in behavior between the two 0.18 µm reported scales [18, 19] are due to the difference in circuit complexity, as shown in Table 7. However, a pattern of behavior is established in short-channel device topologies (65, 55, and 45 nm as in this work) compared to longer channels, including the 90 nm scale topology. This pattern is relatively independent of reported DC supply voltages but heavily dependent on device drain current as a function of drain-to-source voltage.

By combining Table 6 and Table 7 data and comparing the 45 nm scale (this work) with 55 nm scale circuit topologies, we see a power consumption reduction of around 30 times for the 45 nm scale while the TIA gain remains nearly unchanged. A similar result applies when comparing the 45 nm (this work) and 65 nm scale circuit topologies, with a power consumption reduction of around 18 times for the 45 nm scale. This can be explained by the short channel effects impacting the drain current stability performance for the 55 and 65 nm scales in terms of drain-induced barrier lowering (DIBL), where there could have been a considerable overlap between drain-to-source

depletion regions. In the case of the 45 nm scale (this work), the impact was lesser.

In addition, the circuit complexity in terms of the number of passive resistors also plays a role. The 55 nm topology has two passive resistors, while the 65 nm topology has four passive resistors, affecting energy storage compared to the zero passive resistors in the 45 nm scale, highlighting the novelty of this work.

In the circuit topology with long channel devices like the 0.18 µm CMOS [19], a high power consumption of 18 mW is expected given the two spiral inductors used (without the active inductor configuration applied in this work), despite only using six transistors. When comparing the 45 nm scale and the 90 nm scale topologies, the power consumption reduction is slightly less than 3 times for the 45 nm scale, given the unified 1V DC supply voltage for both cases. However, one passive resistor was used in the 90 nm topology [20].

A combination of channel length, circuit design, complexity, and DC supply voltage level can play a crucial role in determining power consumption. For instance, the 55 nm scale topology operates at 2.5V supply voltage and leads to 15 mW of consumption [22], while the 0.18 µm scale topology operates at 1.8V supply voltage and leads to 18 mW of consumption [19].

The real impact of the proposed TIA layout is in its local active inductor feedback, which offers a significant advantage in replacing ordinary spiral inductors, thereby reducing the volume on the chip significantly. In addition, as explained, a reduction in power consumption happens to be as a consequence of this replacement. Further theoretical analysis shows that existing literature does not tackle the feedback loop design problems with the same efficiency as the active inductor feedback reported in this work.

For instance, the range of the active inductor feedback impedance Z_f as in Eq. (18) extends from the DC level magnitude $(1/g_{m11})$ to its magnitude at frequencies up to the f_{-3dB} bandwidth, allowing smarter control over TIA gain, bandwidth, and power consumption. Additional control of Z_f comes at high frequencies when $r_{o12}C_{gs11}s \gg 1$ as well as when $(C_{gs11}s)$ approaches the g_{m11} magnitude. The Z_f pole-zero $\left(-1/r_{o12}C_{gs11}\right)$ cancellation presents an excellent opportunity for future work to achieve even smarter controls.

5. Conclusion

Achieving high TIA gain with extremely low power consumption, moderate input-referred noise, and adequate bandwidth with 1V DC supply voltage is reported. The input stage, which is a current gain provider followed by a TIA gain provider, proved to have important features in circuit design in which a relaxed trade-off occurred between input-referred noise and bandwidth.

Power consumption reduction seemed to extremely alleviate the cycle of trade-offs associated with TIA gain which explains the novelty of this work. Compared to existing literature, a real layout impact based on active inductor feedback is introduced which enabled very low power consumption.

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