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ARTICLE

Optimization of Source Pocket Height on Source Pocket Half Hetero Dielectric Double Gate TFETs (SP-HHD-DG-TFET)

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Abstract: Tunnel field effect transistor (TFET) has attracted significant attention due to its extremely low sub-threshold swing (SS) and leakage current. However, due to the ambipolar effect and relatively low ON-current, researchers are modifying the structures and selecting appropriate materials. In order to increase the ON-current, a highly dense thin layer, source pocket (SP) is used, while a hetero-dielectric gate is used to reduce ambipolar current. Hence, various characteristics, properties, and parameters of the source pocket half hetero-dielectric double gate TFET (SP-HHD-DG-TFET) are studied by varying the SP height (4, 6, and 8 nm) using the Silvaco TCAD simulator. The optimized SP height of 6 nm shows a current ratio (I_{ON}/I_{OFF}) and a sub-threshold swing (SS) to be 3.90×10^{12} and $17.59\ mV/decade$, respectively. Hence, the optimized height and the model are suggested to be useful for low-power and high-speed devices.

Keywords: Sub-threshold Swing (SS), Conductance, Source Pocket (SP), Tunneling, Off–current, On-current, Tunnel field-effect transistor (TFET).

1. Introduction

The tunnel field effect transistor (TFET) is replacing conventional MOSFET due to its small sub-threshold swing (SS), less than $60\ mV/decade$ [1], and low leakage current. Hence, it can be used for low-current and low-power circuits [2]. However, a major disadvantage is the ambipolar current effect, where the n-channel TFET behaves as an 'ON' state instead of an 'OFF' state when a high negative gate bias voltage is applied. Hence, it became difficult to use TFETs in CMOS circuit applications. To address this challenge, various techniques have been explored, such as gate engineering, drain engineering, and spacer/ energy-band engineering.

The 'OFF' state tunneling current is controlled by using an additional gate, called a tunneling gate [3], in the gate engineering technique. Alternatively, using an underlap gate-drain (UGD) in TFETs [2, 4] allows control of channel resistance near the drain channel current. However, both techniques require an additional gate or extra area near the drain. It limits the scalability of the device [5-7]. These challenges of scalability and tunneling current can be overcome by drain engineering, which involves using an undoped (UD) [5, 8, 9] or lightly doped (LD) drain, or introducing a pocket near the drain [10–13]. For instance, Dhiman *et al.* proposed a graded-doped (GD) drain TFET to mitigate the ambipolar effect [14].

On the other hand, Lu et al. [15] mentioned that due to the large and indirect bandgap of Si, Si-TFETs suffer from unacceptably low 'ON'-state currents, below the levels recommended by the International Technology Roadmap for Semiconductors (ITRS) [16,17]. The low 'ON'-current limits the switching speed of the device.

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To overcome this, the use of Heterojunction TFETs (HTFETs), formed by junctions between III–V semiconductors and silicon, has been suggested. For p-channel TFETs, the InAs/Si HTFET has been proposed because of its lower tunneling mass [18], which facilitates the direct tunneling process [19]. The 'ON'-state current can be improved by inserting an ultra-thin doping pocket at the junction between the heavily doped source and the intrinsic channel within the channel region [20, 21], as there will be the formation of steeper energy band bending and a reduction in the tunneling distance.

Energy-band engineering, i.e., using heterojunctions and the novel device structures of source pocket (SP), as done in the drain engineering, is used in a single device, specifically the InAs/Si heterojunction. The use of SP and junction, i.e., the hetero SP-TFET (HSP-TFET), is proposed by Lu *et al*. [15]. The authors have done comparative studies with traditional Si-TFETs and found that the proposed InAs/Si HSP-TFET significantly enhanced device performance.

Instead of using a single gate oxides of Si/Hf, horizontally stacked layers of high-k gate oxides have been shown to enhance multiple device characteristics. The decrease in the ambipolar current, along with SS values to below 5 mV/decade, is found by using SP along with a layer of high-k oxide materials in the gate [22]. Even the current switching ratio (I_{ON}/I_{OFF}) is improved by varying the concentrations of doping and the height of the SP. Wang proposes that the hetero-gate-dielectric (HGD) and SP in a DG TFET enhance I_{ON} and reduce the ambipolar current [23].

Sharma *et al.* showed that an SP of SiGe with hetero oxides gives better electrical characteristics compared to that of normal TFETs, SiO_2-gate oxide TFETs, high-k TFETs, and hetero-dielectric SP TFETs [24]. Kavindra *et al*. [25] also showed that the performance of SP hetero-dielectric double gate TFET (SP-HD-DG-TFET) is found to be better in terms of I-V characteristics, I_{ON}/I_{OFF}, and SS compared with hetero-dielectric double gate TFETs (HD-DG-TFET), high-k TFETs, and conventional DG TFETs.

Using Silvaco TCAD [26], various characteristics of the SP-half hetero-dielectric double gate TFET (SP-HHD- DG-TFET) were studied by varying the SP height. The optimized SP height significantly improves the device's properties, making it suitable for low-power, high-speed applications.

2. Device Structure, Parameters, and Simulation Details

The 2D schematic diagram of the SP-HHD-DG-TFET is shown in Fig. 1. The gate consists of SiO_2 oxide in the half region near the n-doped drain, while the other half—toward the heavily p-doped source—uses hetero high-k dielectrics, specifically HfO_2 and Al_2O_3. Since the gate structure is present on both the top and bottom sides of the channel, the device operates as a double-gate structure, which enhances channel controllability. The channel is composed of intrinsic Si, and a single, highly doped GaAs SP is introduced at the source–channel junction within the channel region. The various physical parameters used in the model are provided in Fig. 1 and summarized in Table 1. All simulations were performed using the Silvaco TCAD tool [26].

TABLE 1. Constant parameters used for simulation.

Doping Concentration (cm^{-3})	
p-type Source (n_s)	1×10^{20}
n-type Channel (n_c)	1×10^{17}
n-type Drain (n_d)	5×10^{18}
n-type SP (n_{SP})	7×10^{18}
Dielectric Constant	
SiO_2	3.9
HfO_2	25
Al_2O_3	8.5
Length of the SP (nm)	2.5
Work function of gate (eV)	4.2

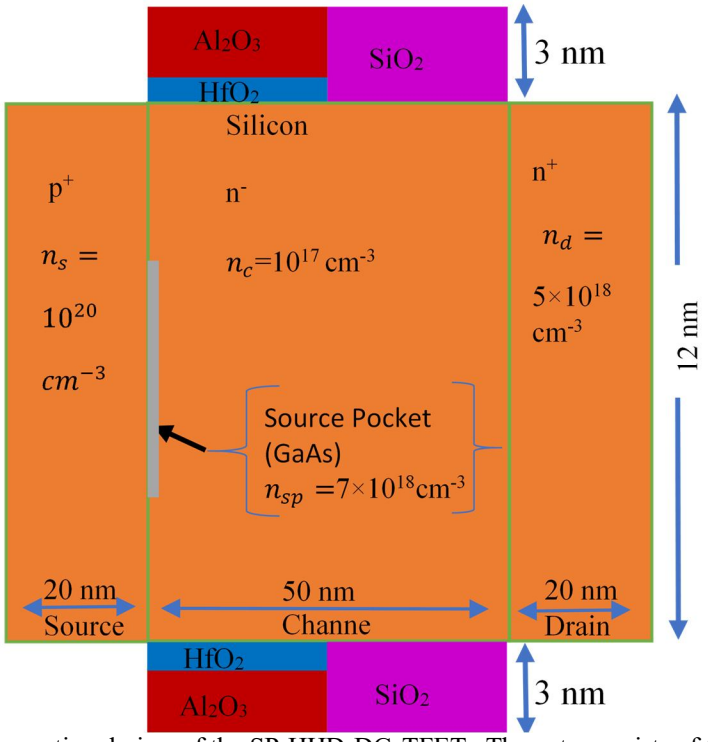

FIG. 1. Schematic cross-sectional view of the SP-HHD-DG-TFET. The gate consists of SiO_2 (3 nm in height) near the drain, and the other half with hetero-dielectrics of HfO_2- Al_2O_3 (1 and 2 nm in height, respectively) is near the source. The p-type source and the n-type drain have concentrations of 1×10^20 cm^-3 and 5×10^18 cm^-3, respectively. n-type SP of $GaAs$ and the channel of Si are with concentrations of $7 \times 10^{18} cm^{-3}$ and $1 \times 10^{17} cm^{-3}$, respectively.

3. Results and Discussion

The 2D simulated structure of SP-HHD-DG-TFET is shown in Fig. 1. The doping concentration of the heavily doped source p^+ of 20 nm in length is 10^{20}cm^{-3}. The nearly intrinsic n-type channel has a doping concentration of 10^{17}cm^{-3} and a length of 50 nm. The n −type doping concentration of SP of GaAl (length 2.5 nm), positioned between the source and the channel, is $7 \times 10^{18}\text{cm}^{-3}$. The n −type drain has a doping concentration of $5 \times 10^{18}\text{cm}^{-3}$ and a length of 20 nm. Work functions of the front gate (Fgate) and back gate (Bgate) are equal (4.2 eV). The gates are made common in the circuit connection, and the work function of the SP is 5.3 eV. All constant parameters are given in Table 1.

In order to optimize the performance of the device, the Silvaco TCAD [26] simulator is used to vary the height of the SP (4, 6, and 8 nm). The obtained simulated characteristics and properties, such as surface potential, electric field intensity, band energy, and the I-V characteristics, are given in Figs. 2, 3, 4, and 5, respectively. The calculated physical parameters of the simulation, such as V_{TH}, I_{ON}, I_{OFF}, (I_{ON}/I_{OFF}) ratio, SS, and trans-conductance (g_m), are given inTable 2.

The variation of surface potential along the channel length at $V_{GS} = V_{DS} = 1$ V is shown in Fig. 2. A sharp increase in surface potential is observed at the source–channel junction. This enhancement occurs because the gate oxide near the source consists of high-k dielectrics (HfO_2 and Al_2O_3), and the heavily doped SP further strengthens the potential. Among the examined SP heights (4 nm, 6 nm, and 8 nm), the maximum surface potential is obtained for the SP height of 6 nm, as illustrated in the inset of Fig. 2.

In contrast, near and within the drain side of the channel, the effect of SP height is insignificant, and the surface potential remains nearly constant. This indicates that the region corresponds to the depletion or space-charge region. Kavi *et al.* [25] also included the drain–channel depletion region in their modeling to achieve accurate device representation in this area.

The electric field distribution, shown in Fig. 3, exhibits a strong peak at the source–channel interface. This is attributed to the high charge

carrier density in the source region as well as in the SP. The presence of high-k hetero-dielectrics (HfO_2 and Al_2O_3) at the gate near the source further contributes to the enhanced electric field. The maximum value at the sharp peak of the electric field is due to the presence of more charge for the SP of 8 nm in height. This peak indicates an increased number of charge carriers tunneling through the junction.

Figure 4 shows the state at $V_{GS} = V_{DS} = 1$ V, i.e., at the 'ON' state. It is known that with n-type and p-type doping, the conduction band energy level decreases and the valence band level increases, respectively, i.e., the Fermi level moves towards the conduction and valence band. Under the unbiased condition, the energy band is not sharp, representing the 'OFF' state. The energy gap increases due to the reverse biasing and becomes sharp, i.e., the higher level of the conduction band energy and the lower level of the valence band energy at the source and drain sides, respectively. will come very close to each other at the channel region due to the band bending. It can be seen in the inset of Fig. 4.

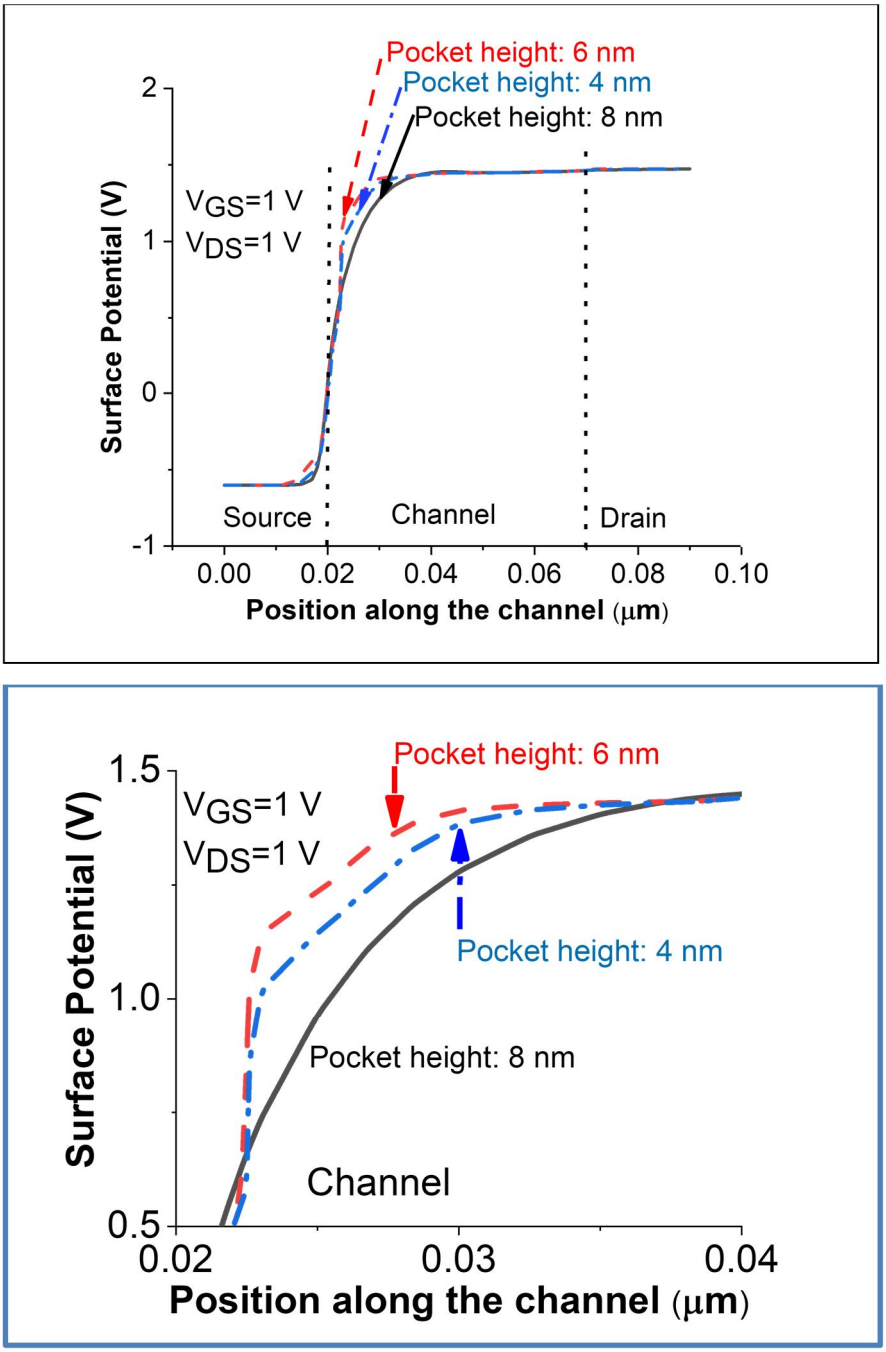

FIG. 2. Surface potential versus the position along the channel for SP heights of 4, 6, and 8 nm at $V_{GS} = V_{DS} = 1\,V$. The inset view highlights the difference in the characteristics.

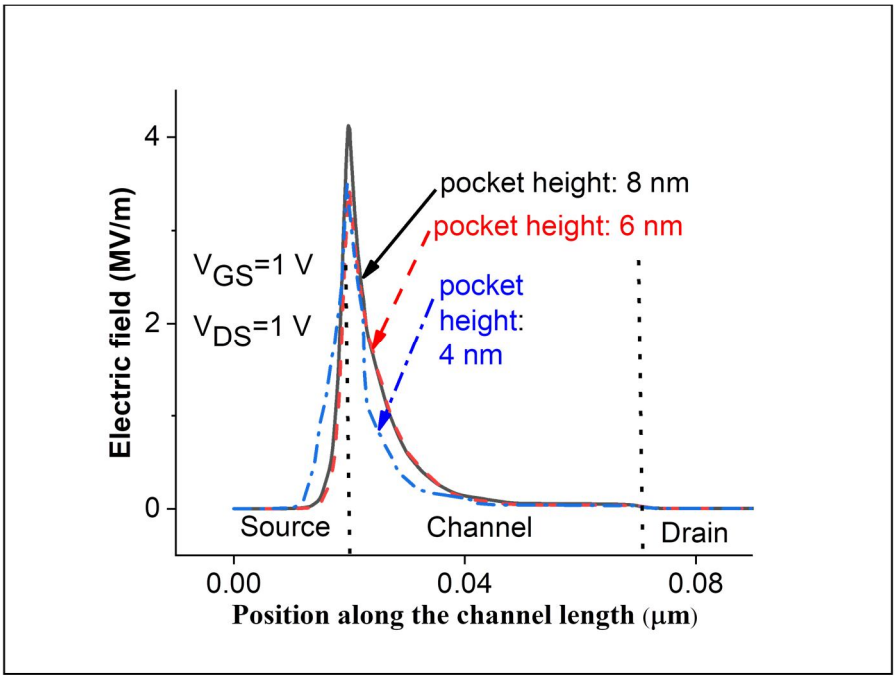

FIG. 3. Electric field versus the position along the channel length for SP heights of 4, 6, and 8 nm at $V_{GS} = V_{DS} = 1\,V$.

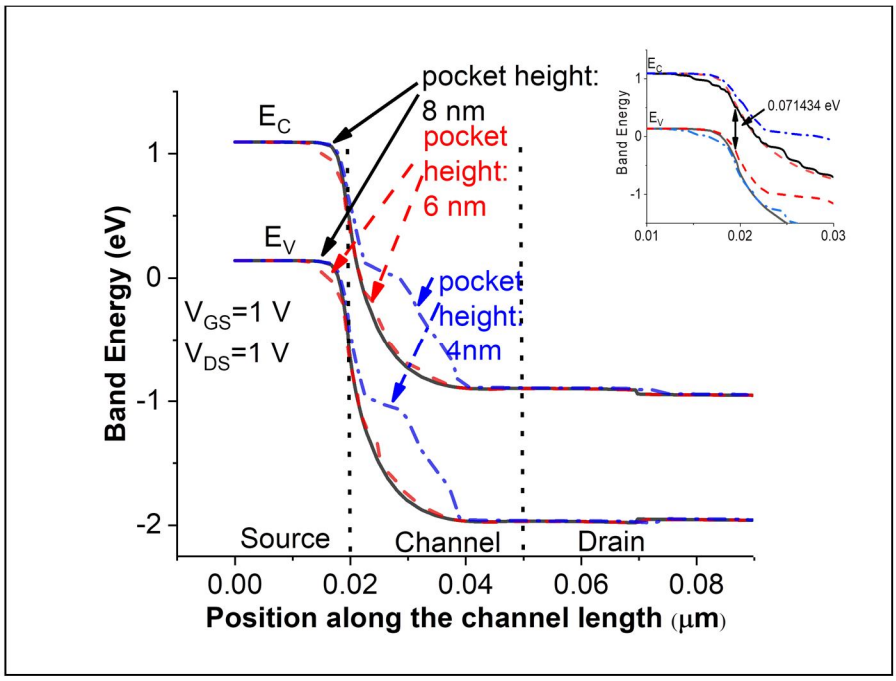

FIG. 4. Band Energy variation versus the position along the channel length for SP heights of 4, 6, and 8 nm at $V_{GS} = V_{DS} = 1\,V$.

At $V_{GS} = 0$, the width of the tunneling channel and the height of the energy band are functions of the doping concentrations. Hence, electrons do not have enough energy to move from the valence band to the conduction band. Whereas, as V_{GS} increases, both the CB and the VB energy differences increase, as is the condition of –ve biasing/reverse bias. Figure 4 shows the energy band diagram under the condition $V_{GS} = V_{DS} = 1$ V, where the energy varies along the effective channel length. With an increase in the gate voltage, more band bending takes place, i.e., the conduction band of the source and valence band of the channel/drain are increased and become sharper, causing a reduction in tunneling length, facilitating faster carrier movement in opposite directions across the source–channel junction, resulting in a higher drain current. At $V_{DS} > V_{Th}$, the electrons move from the valence band to the conduction band as

they have sufficient energy to tunnel. The inter-band tunneling is also due to the bands approaching each other, i.e., the narrowing of the effective length of the channel, corresponding to the ON-state condition. With an increase in the gate voltage, the current increases, as shown in Fig. 5. The inset view of Fig. 4 also shows the maximum narrowing of the effective channel length at $V_{GS} = V_{DS} = 1\,V$, causing such an effect. For the tunneling of the electron from the source to the drain via the channel region, the non-local band-to-band tunnel (BTBT) model is used [14, 27, 28]. Kavi *et al*. mentioned that to recombine the electron-hole pair during conduction through the channel, the Auger recombination and Shockley-Read-Hall recombination models are also used [22]. In addition, the Lombardi model is used to incorporate the effect of doping, electric field, and concentration [22]. Due to the high concentration of doping in the source and drain, compared to that of the channel, the band gap narrowing (BGN) model is incorporated [29, 30]. Collectively, these physical models are included in the simulation to accurately describe the current tunneling phenomena.

The variation of drain current versus reverse/back gate voltage for pocket heights ranging from 4 to 8 nm is given in Fig. 5 at $V_{DS} = 1\,V$. The drain current for the 8 nm pocket height is slightly higher than that for the rest of the heights, which is expected due to the availability of a larger number of carriers as the SP is heavily doped.

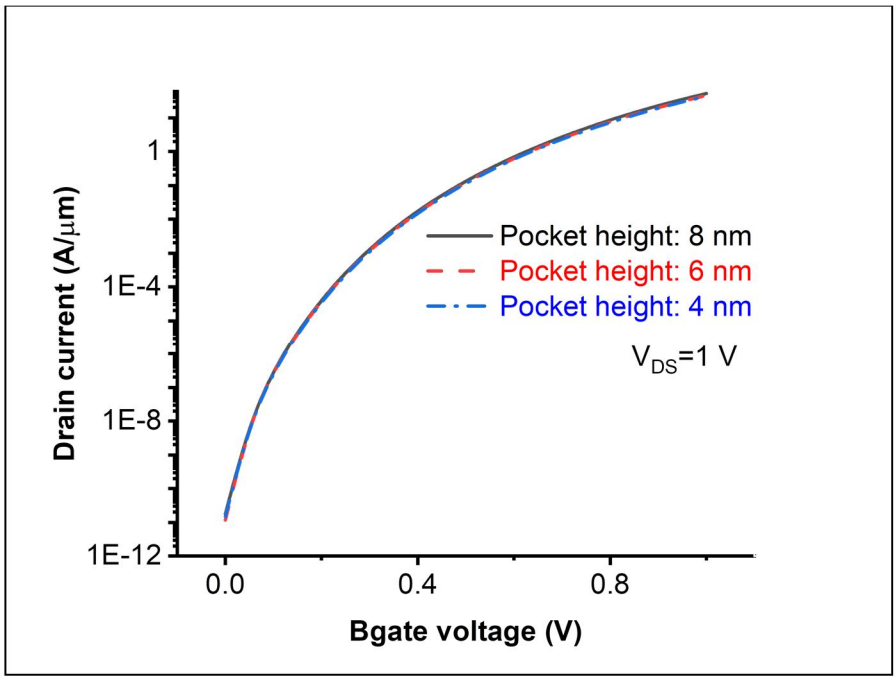

FIG. 5. Variation of drain current versus backward gate (Bgate) voltage for SP heights of 4, 6, and 8 *nm* at $V_{DS} = 1\,V$.

TABLE 2. Physical parameters obtained by simulation with the height of the SP.

S.N.	Parameters	Height of the SP (nm)		
		8	6	4
1.	V_{TH} (V)	0.3465	0.3446	0.3445
2.	I_{ON} (A/μm)	5.20×10^{-5}	4.55×10^{-5}	4.31×10^{-5}
3.	I_{OFF} (A/μm)	1.78×10^{-17}	1.17×10^{-17}	1.48×10^{-17}
4.	I_{ON}/I_{OFF}	2.93×10^{12}	3.90×10^{12}	2.91×10^{12}
5.	Sub-threshold slope	53.62	56.85	54.31
6.	SS (mV/decade)	18.35	17.59	18.41
7.	g_m (Siemen)	$3.39X10^{-4}$	2.93×10^{-4}	2.77×10^{-4}

The threshold voltage (V_{Th}) does not vary significantly with the change in pocket height. I_{ON} decreases with a decrease in the height of the SP, whereas the I_{OFF} decreases and then increases with the height of the SP. However, the current ratio is found to be maximum for the $6\,nm$ height, with a value of 3.90×10^{12}. The current ratio is close to the p-channel SP-HD-DG-TFET, reported at 4.4×10^{12} by Kavi *et al.* [25]. The SS for the $6\,nm$ SP height is $17.59\ \mathrm{mV/decade}$ and found to be the minimum when compared to that of the other heights. The trans-conductance g_m for the height is also found to be lowest, i.e., $2.93 \times 10^{-4}\,S$. So, the optimized height of the SP is expected to be appropriate for a low-power consumption application.

4. Conclusions

Due to the importance of using a SP along with the hetero-dielectrics of high-k materials in a DG-TFET, various electrical characteristics, such as surface potential, electrical energy, bandgap energy, and I-V characteristics, are studied using Silvaco TCAD simulation software.

The calculations of threshold voltage, ON and OFF currents, current ratio, SS, and transconductance are also done.

The variation of such properties and parameters due to the height of the SP on the SP-HHD-DG-TFET is studied/obtained. The SP with the height of 6 nm is found to have the highest current ratio (I_{ON}/I_{OFF}) and the lowest SS. Hence, the optimized height of 6 nm is recommended for low-power and high-frequency applications.

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