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ARTICLE

Modeling and Simulation of Current Voltage Characteristics for Cylindrical CNTFET Transistor

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Abstract: In this study, we present a physics-based analytical model for the current-voltage characteristics of a near-ballistic CNTFET with a single-wall zig-zag carbon nanotube (16, 0). This model is based on the calculation of the potential and threshold voltage in the channel of a cylindrical gate CNTFET. Consequently, a new expression for the mobility law as a function of the CNT geometric parameters is proposed. Subsequently, a new model of I-V characteristics is presented, accounting for the impact of edge resistances. The paper also discusses the DIBL, subthreshold slope (SS), and the impact of some geometric and physical parameters on the drain current. A comparison of the I-V characteristics shows a good agreement between our model and the FETToy model.

Keywords: Cylindrical gate CNTFET, I-V characteristics, Threshold voltage, Analytical model, Mobility law.

1. Introduction

Since the discovery of carbon nanotubes (CNT) by Iijima in 1991 [1] and the fabrication of the first field-effect transistor based on carbon nanotubes (CNTFET) in 1998 [2, 3], CNTFET transistors have been considered promising for high-speed applications due to their quasi-ballistic properties and high Fermi velocity (10^6m/s) [4]. CNTFETs are among the top candidates to complement CMOS technology. Single-walled carbon nanotubes (SWNTs) are used as the channel material in carbon nanotube field effect transistors (CNTFETs). The structure of a CNTFET is similar to MOSFET, with the channel between the source and drain electrodes replaced by a carbon nanotube. CNTFETs exhibit excellent carrier mobility and utilize a high-quality gate dielectric [5]. In this paper, we have developed a physics-based analytical model for a cylindrical gate CNTFET. By using the potential fluctuations between the gate and the carbon nanotube, we have introduced a simple relationship between the potential under-gate voltage (V_{gcnt}), the CNT surface potential (V_{cnt}), and the barrier between the gate electrode and the CNT surface (V_{cb}) [6]. Then, we developed a new model for the current-voltage characteristics of a CNTFET with a coaxial structure. The model is based on a new mobility law, which is variable and depends on the length and diameter of the CNT, as well as on the electric field fluctuations in the channel. This mobility law in our model corresponds to both the quasi-ballistic regime and the effects of a very short channel. The model also takes into account the impact of parasitic resistances at the edges of the channel, which reduce the voltage applied between the drain and the source. After that, we created simulation software to explore the I-V characteristics of the device, highlighting the influence of various physical and geometrical parameters (such as CNT length and diameter, oxide thickness, work function, oxide

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permittivity, and series resistances). A comparison between the I-V characteristics of our model and those from the FETToy simulator in the literature [7] was conducted for a transistor with a gate length of 20nm. The close agreement between the two sets of results demonstrates the effectiveness of our model.

2. Presentation of the Model

2.1 Device Structure

CNTFET transistors have structures like MOSFET, where the semiconductor channel between the source and drain electrodes is replaced by the carbon nanotube CNT. The cylindrical gate CNTFET is a special structure of CNTFETs due to its geometry (Fig. 1). This device exhibits a wraparound gate that maximizes the capacitive coupling between the gate and the CNT channel [8, 9]. In this paper, the channel of the proposed device is formed with a single-wall zig-zag semiconductor nanotube (16,0) which has a diameter of 1.25 nm and a length of 20 nm. The source and drain electrodes are placed at the edges of the nanotube, while the gate electrode is coaxially placed along the tube axis. The spaces between the gate and the source and between the gate and the drain are n-type doped semiconductors. Source and drain electrodes are made of palladium (Pd). The gate metal, which is cobalt (Co), forms a Schottky barrier with the CNT semiconductor. The dielectric oxide used for gate insulation is silicon dioxide (SiO_2). V_{GS} is the voltage applied to the gate and V_{DS} is the voltage applied to the drain.

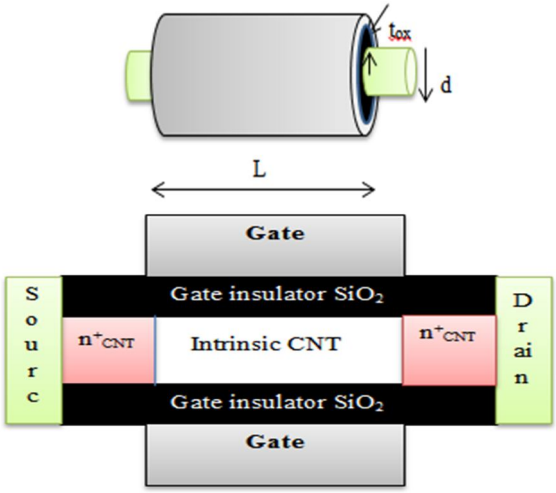


FIG. 1. Structure of the coaxial CNTEFT.

2.2 Potential Distribution

To calculate the potential under the gate, we rely on the work of J. M. Marulanda *et al*. [6] and B. N. Kumar [10], making specific adjustments for the cylindrical structure.

According to [6] and [10], the potential distribution between the gate electrode and the carbon nanotube is given by,

$$V_{gcnt} = \phi_{mc} - \psi_{OX} + \psi_{cnt} \quad (1)$$

Where:

Φ_{mc} is the work function difference between the gate electrode and the carbon nanotube, it is given by:

$$\phi_{mc} = \phi_m - \phi_c \quad (2)$$

ψ_{OX} is the voltage across the oxide, given by:

$$\psi_{OX} = \frac{Q_{OX}}{C_{OX}} \quad (3)$$

ψ_{cnt} is the surface potential at the interface between the gate oxide and the carbon nanotube, given by:

$$\psi_{cnt} = V_{cnt} - \frac{\Delta E_F}{q} + \frac{E_c}{q} - \frac{KT}{q} \quad (4)$$

Flat band voltage is defined as follows:

$$V_{fb} = \phi_{mc} - \frac{Q_{OX}}{C_{OX}} \quad (5)$$

So, the expression for the gate voltage can be given as:

$$V_{gcnt} = V_{fb} + V_{cnt} - \frac{\Delta E_F}{q} + \frac{E_C}{q} - \frac{KT}{q} \quad (6)$$

The difference in Fermi levels between the doped regions (source and drain sides) and the channel (intrinsic CNT) is given by:

$$\Delta E_F = KTln(1 + \frac{N_d}{n_i}) \quad (7)$$

Here, N_d is the carrier concentration, n_i is the CNT intrinsic concentration, K is the Boltzmann constant, and T is the temperature.

The conduction band is expressed as follows [11]:

$$E_C = \Delta_1 - qV_{cnt} \quad (8)$$

$$\Delta_1 = \frac{E_G}{2} = \frac{a_{V_{pp\pi}}}{d\sqrt{3}}$$

The modulated potential V_{cnt} in the carbon nanotube field effect transistors can be given as follows [10]:

$$V_{cnt} = V_{GS} - \alpha \frac{Q_0}{C_{OX}} \quad (9)$$

$$Q_0 = qn_iL \quad (10)$$

$$\alpha = ln\left[1 + \lambda\left(\frac{V_{DS}}{V_t}\right)\right]\left(1 - \exp\left(\frac{-qV_{GS}}{KT}\right)\right) \quad (11)$$

λ: is a fitting parameter.

The intrinsic carrier density expression is given by [12]:

$$n_i = \left[\frac{4\sqrt{KTE_g}}{(3\sqrt{\pi}a_{cc}V_{pp\pi})}\right] e^{\left(\frac{E_g}{2KT}\right)} \quad (12)$$

Here, a_{cc} is the nearest neighbor distance between C-C bonds and $V_{pp\pi}$ is the energy transfer integral for carbon nanotubes.

2.3. I-V Model

The drain-source current characteristic for a CNTFET with a short channel is described by the following formula [6, 10]:

$$I_{DS} = \beta[f\{\psi_{cnt}(L), V_{GS}\} - f\{\psi_{cnt}(0), V_{GS}\}] \quad (13)$$

Where:

$$f\{\psi_{cnt}(x), V_{gs}\} = \left(V_{GS} + V_{sb} - V_{fb} + \frac{KT}{q}\right)\psi_{cnt}(x) - \frac{1}{2}{\psi_{cnt}}^2(x) \quad (14)$$

For cylindrical structure CNTFET, β is given by:

$$\beta = \frac{\gamma\mu C_{Ox}}{L^2} \quad (15)$$

Here, the gate oxide capacitance is given by:

$$C_{ox} = \frac{2\pi L\varepsilon_0\varepsilon_r}{log\left(\frac{r+t_{ox}}{r}\right)} \quad (16)$$

Where r is CNT radius ($r = d/2$), t_{ox} is the oxide thickness, $\varepsilon_0\varepsilon_r$ is the oxide permittivity and γ is an adjustable coefficient, in our model $\gamma = 0.97$, μ is the carrier mobility.

In short-channel devices, carrier mobility is not constant; rather, it depends on the length and diameter of the carbon nanotube (CNT). This is attributed to quasi-ballistic transport. Additionally, carrier mobility is influenced by the electric field variation in the channel. As the electric field increases, mobility tends to decrease. Moreover, there is a saturation of velocity, leading to a decrease in mobility and saturation of the drain current.

In this model, an empirical expression of the mobility is given as follows:

$$\mu = \mu_0\left(\frac{L}{(L+L_\mu)}\right)\left(\frac{d}{(d+d_\mu)}\right)\left(1/\sqrt{1 + \left(\frac{E}{E_\mu}\right)^2}\right) \quad (17)$$

Where

$\mu_0 = 1350\ cm^2/V.s$

$L_\mu = 100nm$

$d_\mu = 0.2\ nm$

E is the electric field, $E = V_{ds}/L$

$E_\mu = 2.5.10^5 V/cm$

The current voltage expression can be divided into two regimes: linear and saturation.

Drain current in the linear regime of CNTFET can be described as follows:

$$I_{DS,ln} = \beta\left[\left(V_{GS} - V_{Th} + \frac{KT}{q}\right)V_{ds} - \frac{V_{ds}^2}{2}\right] \quad (18)$$

We can also obtain the saturation drain current by replacing $V_{GS} - V_{Th}$ by $V_{DS,st}$, then the current expression in the saturation regime becomes as:

$$I_{DS,st} = \beta\left[\left(V_{ds,st} + \frac{KT}{q}\right)V_{ds,st} - \frac{V_{ds,st}^2}{2}\right] \quad (19)$$

Where V_{Th} is the threshold voltage, by definition, is the voltage at which the channel begins to conduct. Therefore, the threshold voltage can be expressed as:

$$V_{Th} = V_{fb} - \frac{\Delta E_F}{q} + \frac{E_C}{q} - \frac{KT}{q} \quad (20)$$

In this model, we are also interested in the DIBL (drain-induced barrier lowering) and in the subthreshold swing (SS).

The DIBL is a short-channel effect in CNTFETs and MOSFETs results in a reduction

of threshold voltage [13-14]. The DIBL is defined by:

$$DIBL = \frac{\Delta V_{Th}}{\Delta V_{DS}} \quad (21)$$

The subthreshold slope (SS) stands out as a crucial performance parameter for transistors. A small subthreshold slope is essential to ensure a satisfactory on/off current ratio. It is also highly desirable for achieving low threshold voltage and enabling low-power operation, especially as FETs are scaled down to small sizes [14, 15]. The subthreshold slope is given by:

$$SS = \left(\frac{d\,V_{GS}}{d\,log I_{DS}}\right) \quad (22)$$

2.4 Parasitic Resistance Effect

The parasitic resistances consist of two components: the carbon nanotube extension resistances and the metal-CNT contact resistances [16, 17]. These include resistances at the channel edges on the source side (R_S) and the drain side (R_D). While several models neglect the effect of parasitic resistances, this model introduces the effects of parasitic resistances on the drain voltage value V_{ds}. The impact is proportional to the drain current I_{DS}. To consider the effect of R_S and R_D, we replace the intrinsic drain voltage V_{ds} in Eqs. (18) and (19) with the extrinsic drain voltage V_{DS}, as shown in the following expression:

$$V_{DS} = V_{ds} + (R_S + R_D)I_{DS} \quad (23)$$

3. Results and Discussion

Based on the mathematical study presented in the second part, simulation software written in Fortran 90 has been developed. This software enables the solution of the system of mathematical equations and the extraction of various tables of values. The Origin software was used to draw the different series of curves.

To check the validity of our model, we present in this section a comparison between the I_{DS}-V_{DS} characteristics of our model and those of the FETToy simulator, as published by Rechem *et al*. [7] in 2016. The results from the FETToy simulator are considered as reference values. The comparison is made for a coaxial CNTFET with the parameters presented in Table 1.

TABLE 1. Parameters and physical constants used in the simulation.

Parameter	Value
Gate Length (L_G)	20 nm
CNT diameter (d)	1.25 nm
CNT work function	4.5 eV
CNT electron affinity	4.27 eV
CNT energy gap	0.568 eV
Intrinsic concentration (n_i)	$2.35.10^2$ cm^{-1}
$V_{pp\pi}$ Energy transfer integral for carbon nanotubes [18, 19].	2.5eV
Oxide thickness (t_{OX})	2 nm
Oxide relative permittivity ε_r (SiO_2)	3.9
Gate work function (Co)	5.0 eV
Donors concentration (N_d)	10^7 cm^{-1}
Temperature	300K

Figure 2 presents the comparison for gate voltages (V_{GS} = 0.8, 1.0, and 1.2 V). It is clear that the two models are in good agreement. For V_{GS} = 1.0 V and 1.2 V, the error does not exceed 10% in the linear regime, whereas in the saturation regime, there is a perfect correspondence. However, for V_{GS} = 0.8V, the error reaches 20% at V_{DS} = *0.1V* and *0.2V*, while in the saturation regime, there is a correspondence.

The simulation results in this section consider the values of the parameters indicated in Table 1.

The drain current-gate voltage characteristics (I_{DS}–V_{GS}) for different drain voltages (V_{DS}= 0.2 V, 0.4 V, 0.6 V, and 0.8 V) are shown in Fig. 3. It can be observed that when V_{GS} is less than the threshold voltage $V_{Th,}$ (in this case $V_{Th} \approx 0.2$ *V*), the current tends to zero. However, for V_{GS} greater than $V_{Th,}$ the current increases with an increase in both V_{GS} and V_{DS}. This is attributed to the application of a positive gate voltage inducing a heavy charge on the channel. As a result, the drain current increases with the rising gate voltage under the influence of an applied drain voltage.

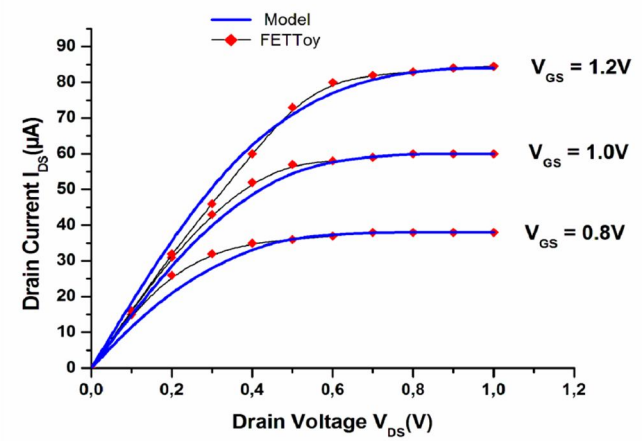


FIG. 2. Comparison of I_{DS}–V_{DS} characteristics between our model and the FETToy model obtained from [7].

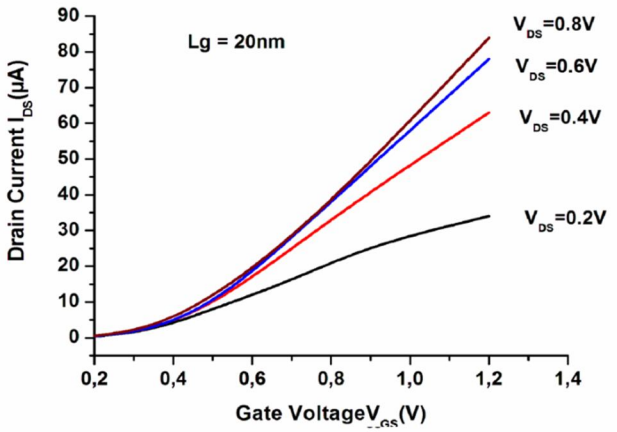


FIG. 3. I_{DS}–V_{GS} characteristics.

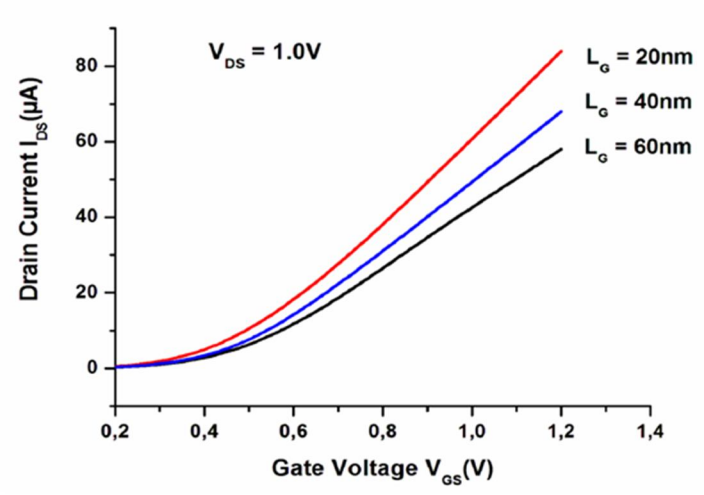
In the subsequent analysis, we studied the impact of some parameters (gate length, oxide relative permittivity, and gate work function) on I-V characteristics, threshold voltage, DIBL, and SS for CNTEFT, whose parameters are shown in Table 1. Each parameter has an individual impact. To study the impact of each parameter, we changed its value and fixed all other parameters.

Figures 4(a) and 4(b) show the impact of the gate length L_G on SW-CNTFET characteristics: Fig. 4(a) presents I_{DS}-V_{GS} characteristics for V_{DS} = 1.0 V and Fig. 4(b) presents I_{DS}-V_{DS} characteristics for V_{GS} = 1.0 V, in both cases the gate length is changed between 20, 40, and 60 nm. We see that for both figures, when gate length L_G = 60 nm, the drain current is smaller, however, it is greater when gate length L_G = 20 nm. For example, when the value of drain current is V_{GS} = 1.0 V and V_{DS} = 1.0V, we find that I_{DS} = 42 nm for L_G = 60 nm, I_{DS} = 49 nm for L_G = 40 nm, and I_{DS} = 60 nm for L_G = 20 nm. This is similar to all FET devices.

The impact of the parasitic resistances at the edges of the channel R_S on the source side and R_D on the drain side on the I-V characteristics is shown in Fig. 5. In our simulation, we took R_S= R_D = 600Ω. These resistances lead to a decrease in the voltage applied to the drain. We can notice that this impact is very important, especially in the cases where V_{GS} = 1.2 V or V_{GS} =1.0 V. The negligence of this impact will involve a significant deformation of the curves, as neglecting these resistances and considering them non-existent is incorrect and damages the credibility of the model. These resistances cannot therefore be neglected in all the modeling and simulations of carbon nanotube transistors.

In our simulation, SiO_2 is used as an oxide between the gate and the CNT, while Co is used as a gate metal, but other materials (oxides and metals) can be used for better performance. Figure 6 presents the saturation drain current as a function of the relative permittivity of some oxides, with their values obtained from [20]. It can be seen that the saturation current increases as the permittivity increases, it has the highest value of 1130 mA for TiO_2 and the smallest value for SiO_2.

(a)



(b)

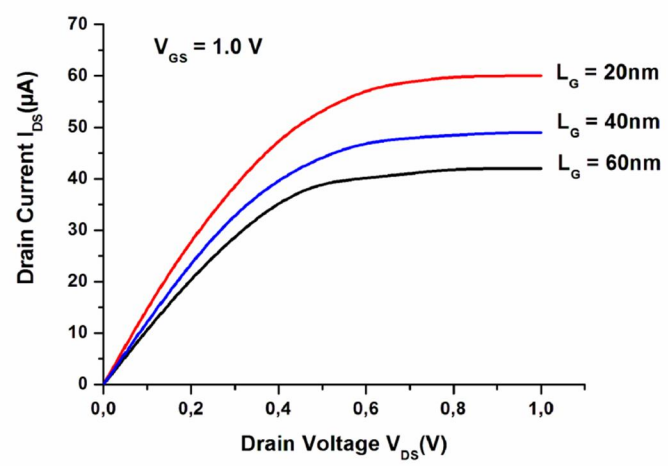


FIG. 4. Impact of gate length on I-V characteristics.

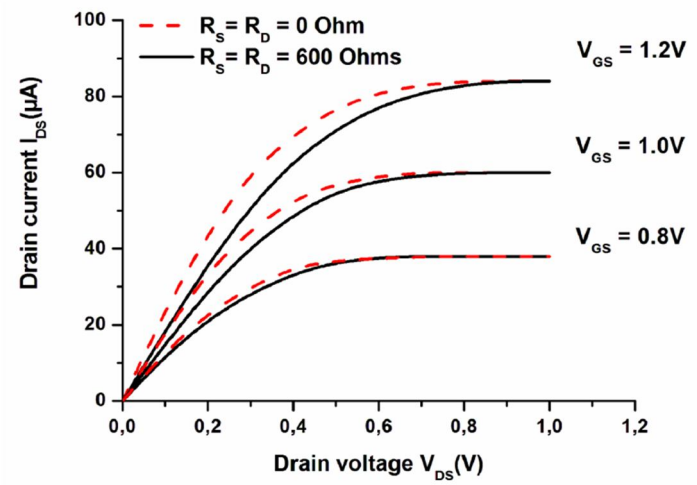


FIG. 5. Impact of parasitic resistances on the I_{DS}-V_{DS} characteristics, R_S=R_D=600KΩ.

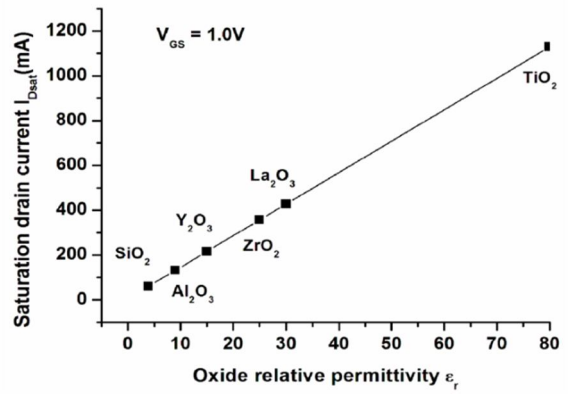


FIG. 6. Effect of oxide relative permittivity (ε_r) on saturation drain current I_{DSs} for V_{GS} = *1.0V.*

Figure 7 shows the impact of the work function of the gate metal on the saturation drain current. The metalwork function values are obtained from [21, 22]. From the curve, it can be seen that the current decreases as the gate work function increases. In this case, the minimum value of the gate work function gives the highest value of the saturation current. This observation suggests that the gate metal's work function acts as a potential barrier, leading to an increase in the threshold voltage and a decrease in the drain current.

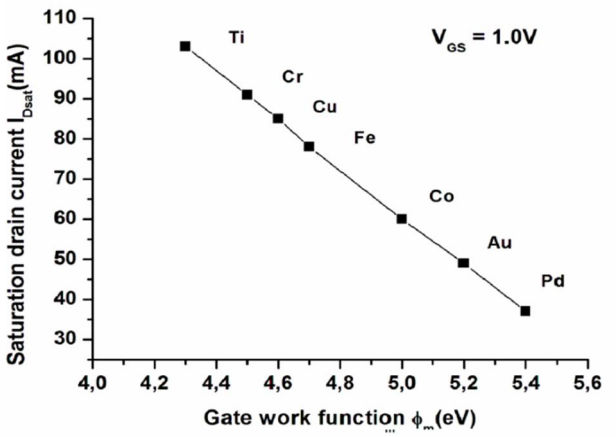


FIG. 7. Effect of gate work function (Φ_m) on the saturation drain current I_{DS} for V_{GS} = *1.0 V.*

Figure 8 shows the variation in the threshold voltage as a function of the relative permittivity of the oxide. From the figure, it is clear that for oxides with small ε_r, there is a linear increase in threshold voltage with an increase of ε_r, while for oxides with great ε_r, there is quasi-saturation of the threshold voltage. To reduce the threshold voltage, it is necessary to use dielectric materials where is low, such as SiO_2 where ε_r = 3.9.

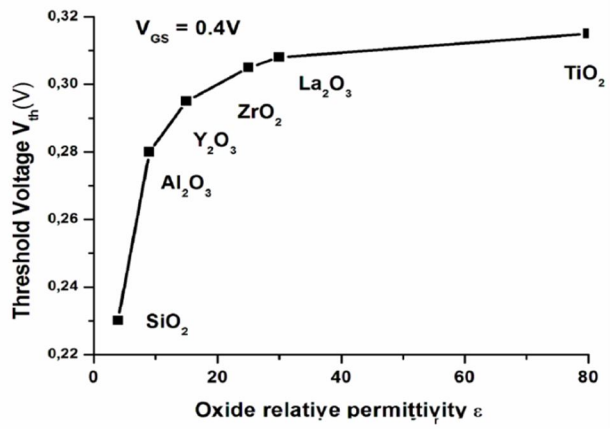


FIG. 8. Impact of the oxide relative permittivity ε_r on the threshold voltage V_{Th} at V_{GS} = *0.4V.*

In Fig. 9, we have presented the impact of the gate work function ϕ_m on the threshold voltage V_{th} at V_{GS} = 0.4 V. The graph reveals a linear increase in the gate work function with the threshold voltage. This relationship is attributed to the difference in work function between the gate metal and the CNT, representing an energy barrier that must be overcome. As the potential barrier increases, so does the threshold voltage. From the figure, we have noted that palladium Pd (ϕ_m = 5.4e V) corresponds to the highest threshold voltage V_{th} = 0.43 V, while titanium Ti (ϕ_m = 4.3e V) corresponds to the lowest threshold voltage V_{th} = - 0.47 V. In our simulation, we used cobalt Co with work function (ϕ_m = 5.0e V), where the threshold voltage V_{th} = 0.23 V.

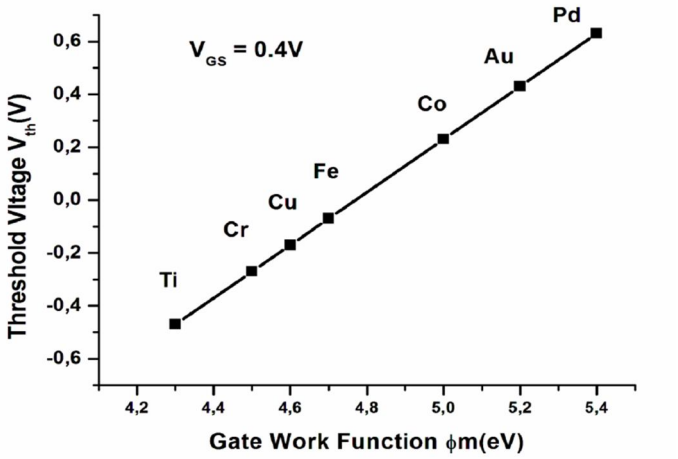


FIG. 9. Impact of the gate work function (Φ_m) on the threshold voltage (V_{Th}) for V_{GS} = *0.4 V.*

Figure 10 shows the DIBL as a function of oxide relative permittivity at a gate voltage V_{GS} = 0.4 V. Initially, it is clear that the DIBL has small values for all oxides, indicating an advantage of this nanoscale device. The curve reveals an exponential decrease in DIBL with an increase in oxide relative permittivity. The maximum value of the DIBL (0,018 mV/V) corresponds to SiO_2 where ε_r = 3.9, then it is decreased to 0.001 mV/V for TiO_2 where ε_r = 80.

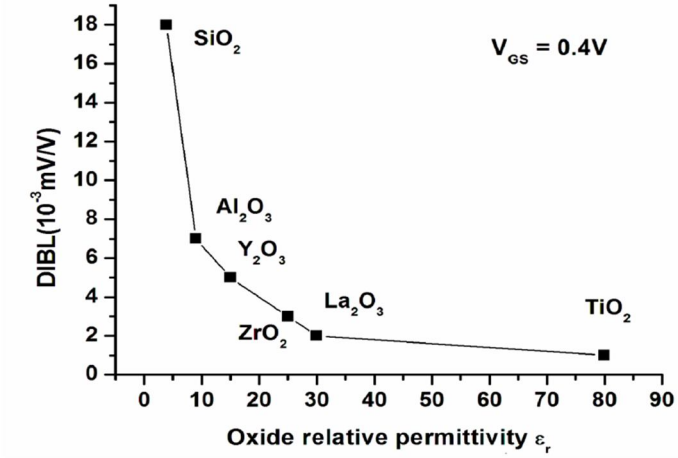


FIG. 10. DIBL versus oxide relative permittivity (ε_r).

In Fig. 11, the subthreshold slope (SS) is plotted against oxide relative permittivity for a gate voltage V_{GS} = 0.4 V and drain voltage V_{DS} = 1.0 V, The SS decreases as the oxide relative permittivity increases, with a maximum value of 178 mV/dec corresponding to ε_r = 3.9 for SiO_2. Subsequently, the SS decreases to 101 mV/dec for TiO_2 (ε_r = *80*). This result suggests that oxides with higher relative permittivity are preferable for limiting the DIBL and SS effects. In general, cylindrical CNTFET devices exhibit good SS and DIBL characteristics.

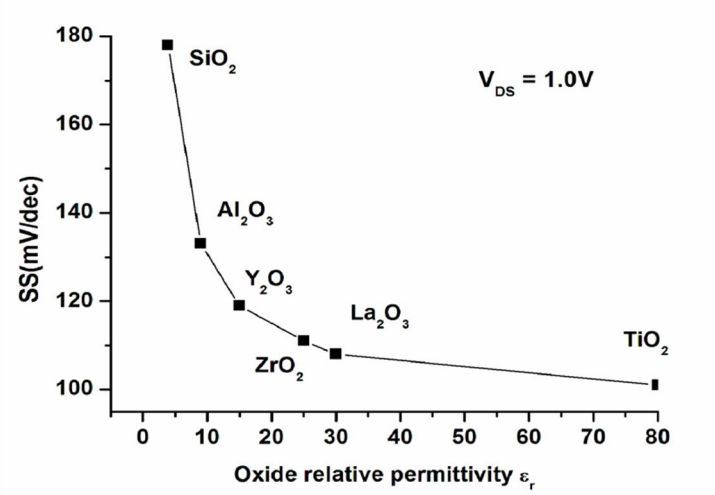


FIG. 11. Subthreshold slope (SS) versus oxide relative permittivity ε_r.

4. Conclusion

In this paper, a physics-based analytical model of I-V characteristics for the CNTFET cylindrical gate is proposed. The model is based on: (1) calculating sub-gate potential and threshold voltage, (2) proposing a new mobility law, and (3) taking into account the impact of parasitic resistances on the I-V characteristics. After the presentation of the analytical study, a simulation software has been developed. I-V characteristics obtained by the model have been validated by comparison with the numerical simulator FETToy, where a good agreement between the two results is shown. The simulation results also included the impact of some parameters such as gate length, relative oxide permittivity and work function of gate metal on the I-V characteristics, threshold voltage, DIBL, and SS. The discussion of the results highlights several key findings: (i) acknowledging the impact of parasitic resistances where we cannot neglect it is crucial, (ii) shorter gate length causes an increase in the drain current, (iii) oxides with lower relative permittivity decrease threshold voltage and saturation current but increase DIBL and subthreshold slope, (iv) gate metals with smaller work functions increase drain current and decrease threshold voltage. To summarize the simulation results of this study, it can be said that for better performance, it is advisable to reduce the gate length, use oxides with high permittivity, and utilize gate metals with smaller work functions. We believe that this study contributes to a better understanding of the physics of the coaxial gate CNTFET and provides insights into the impact of various parameters on device performance.

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